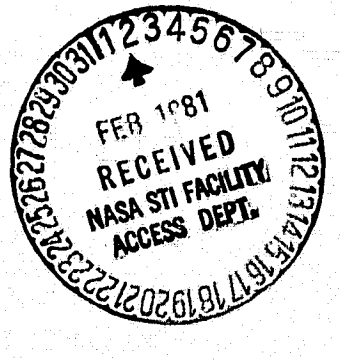
MCR-80-615
Contract NAS8-33194

Final
Report

December 1980

Study of Digital Charge Coupled Devices



MARTIN MARIETTA

MCR-80-615

Contract NAS8-33194

Final Report

December 1980

STUDY OF DIGITAL CHARGE COUPLED DEVICES

Authors:

D. D. Wilson
V.F. Young

Approved:

D.D. Wilson
Program Manager

F. Villella
L. Hamiter
NASA/MSFC Technical Monitors

Prepared for:

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama

MARTIN MARIETTA CORPORATION
DENVER AEROSPACE
Denver, Colorado 80201

FOREWORD

The objective of this study of Digital Charge Coupled Devices was to evaluate the reliability of two shift registers utilizing the charge coupled technology. The Reticon R5101 is a 2000 stage surface channel charge coupled device (SCCD). The Fairchild CCD321A-2 is a dual 455 stage or single 910 stage buried channel charge coupled device. These devices were selected as representative of two CCD processes using the N channel silicon gate MOS technology.

The work was performed under contract NAS8-33194 for the National Aeronautics and Space Administration, Marshall Space Flight Center. The NASA Technical Monitors were Mr. Leon Hamitor and Mr. Felminio Villella. All work was performed at Denver Aerospace of the Martin Marietta Corporation by the parts evaluation and failure analysis laboratories.

The authors thank the Fairchild Semiconductor personnel and the Reticon personnel for their technical support during this study.

CONTENTS

I. Introduction 1

II. Program Definition 3

A. Test Objectives 3

B. Test Methods 3

III. Introduction to CCDs 9

A. CCD Principles 9

B. Surface Channel CCD 9

C. Buried Channel CCD 11

D. Comparison of SCCD and BCCD 15

E. Applications 15

IV. Reticon R5101 19

A. Physical Construction 19

B. Electrical Characterization-General 65

C. Initial Electrical Characterization 84

D. Environmental Screen Tests 88

E. Thermal Step Stress 93

F. Life Test 98

G. Temperature Cycle 105

H. Overvoltage 105

I. Data Analysis 105

J. Failure Analysis 121

K. Conclusions and Recommendations 143

V. Fairchild CCD321A-2 149

A. Physical Construction 149

B. Electrical Characterization-General 180

C. Initial Electrical Characterization 201

D. Environmental Screen Tests 205

E. Thermal Step Stress 207

F. Life Test 208

G. Temperature Cycle 219

H. Overvoltage 219

I. Data Analysis 222

J. Failure Analysis 233

K. Conclusions and Recommendations 249

VI. Appendix 253

ABSTRACT

Charge coupled devices represent unique usage of the Metal-Oxide-Semiconductor concept. These devices can sample an AC signal at the input, transfer charge proportional to this signal through the CCD shift register and then provide an output of the same frequency and shape as the input. The delay time between input and output is controlled by the CCD operating frequency and the number of stages in the shift resister. This work is a reliability evaluation of the Buried Channel and Surface Channel CCD technologies. The constructions are analyzed, failure modes are described, and test results are reported.

I. Introduction

A tremendous amount of work has been done on Charge Coupled Devices since their invention by Bell Laboratories in 1970. There is, however, little information as to the long term reliability of these devices especially as related to space applications.

The work herein provides a discussion of CCD principles and an evaluation of the construction and reliability of the Reticon R5101 and the Fairchild CCD321A-2.

This report will show that these two CCD technologies are reliable and that they have stable parameter characteristics with long term operation. An initial screening program is required to obtain reliable devices with the desired operating characteristics.

II. Program Definition

This program was performed to obtain reliability information on two CCD technologies. The two technologies were compared to determine if either had an inherent advantage for long term space applications. These two technologies were investigated by selecting one part type from each group and performing construction analysis, environmental stress, and high temperature life testing.

A. Test Objectives

1. Assess the design strengths and weaknesses.

2. Determine the most likely failure modes.

3. Develop electrical measurements which can be used to evaluate the operating performance of the devices.

4 Develop optimized burn-in circuits.

5. Identify changes to upgrade the reliability of CCDs for use in space applications.

6. Make recommendations relative to selecting, testing, screening, and applying CCDs.

7. Document design, test, and procurement requirements and provide application and derating guidelines of the use of CCDs.

8. Investigate the high temperature degradation of charge transfer efficiency reported to be caused by hot electron injection.

B. Test Methods

1. Construction Analysis

Two units of each type were analyzed to gain a better understanding of the physical construction so that electrical characteristics could better be understood, failure isolation would be facilitated, and reliability problems could be identified. The following sequence of tests was run:

a. Pin-to-pin electrical characterization for reference during failure analysis.

b. C-V plots

c. Residual gas analysis

d. Microsection one unit of each type

e. Sequentially strip one unit of each type and examine the individual layers.

2. Electrical Characterization

Electrical measurements were performed numerous times during the course of this testing. Initial characterization was performed at -25 °C, +25 °C, and +55 °C. This included measurements of device current, input gate leakage, voltage offset, voltage gain, noise, bandwidth, and transfer efficiency. Full electrical measurement was also performed following the environmental screen tests and following the 4,000 hour life test. Interim electrical measurements, which does not include noise, bandwidth, and transfer efficiency, were made at specified intervals during this study.

A description of the electrical tests follows:

a. Device Power - This is a measure of the current(s) which flow into the parts. For the R5101 this is the current supplied to the clock generator/drivers and that supplied to the output circuitry. For the CCD321A-2 this current is for the output amplifier only. Layer-to-layer shorts or threshold voltage shifts will be indicated if this current level changes.

b. Input Gate Leakage - All of the input gates are checked for current leakage to ground. Due to the number of gates included for a CCD this is a prominent failure mode. This measurement will detect leakage paths in the thermal oxide separating the polysilicon gates from the substrate, leakage paths in the input protection network, and leakage paths between a portion of the overlapping polysilicon layers.

c. Voltage Offset - This measurement is the output amplifier voltage level with no charge being introduced into the channel. The charge which does reach the output amplifier is the thermally generated minority charge. This doubles for every 8 to 10°C temperature increase. An excessive change in this level with operating life could impair the dynamic range of the output signal. An increase in this thermally generated signal could also result in a decrease in the minimum operating frequency.

d. Voltage Gain - This parameter is measured by recording the change in output voltage level for a known change in the input voltage level. The gain is a function of the input circuit sensitivity, the transfer efficiency and the output amplifier gain.

e. Noise - There are many sources of noise in a CCD. There can be input circuit (KT/C_{IN}) charging noise, reset circuit (KT/C_{OUT}) charging noise, output amplifier noise and surface and bulk state trapping noise along the shift register. The RMS voltage level of the output for a fixed input level provides this noise measurement.

f. Bandwidth - The bandwidth is measured by applying a sine wave to the input and measuring the 3 db point on the sampled output. The clock frequency used is as specified in the data sheets. The bandwidth test is both a measure of the upper clocking frequency and the input and output circuit parameters.

g. Transfer Efficiency - This is one of the fundamental parameters for CCDs since it is a measure of several processing and material effects. This test is performed by injecting a logic one during one clock interval and observing the output after it has been shifted through the register. A very accurate determination of the inefficiency can be made by measuring the increase in the next successive analog output and dividing by the number of stages in the shift register.

3. Environmental Screening Tests

Prior to the 4,000 hour life test the parts were screened via tests selected from MIL-STD-883, Method 5004, Class B. The 160 hour burn-in temperature was lowered to +55°C since the effects of high temperature on these CCDs was not known. The tests performed are as listed below:

a. Stabilization bake, Method 1008, Condition C, 24 hours at 150°C.

b. Temperature cycling, Method 1010, -65°C to +150°C.

c. Constant acceleration, Method 2001, 30,000 G, Y1 orientation only.

d. Seal Test - Fine per Method 1014, Condition A, Gross per Method 1014 Condition C.

e. Burn-in, Method 1015, 160 hours at 55°C.

f. External visual, Method 2009.

Following the seal test, interim electricals were performed, and following the burn-in test full electricals were performed.

4. Thermal Step Stress

To determine the temperature to be utilized for the 4,000 hour life test a thermal step stress program was performed. This test was designed to determine the temperature at which catastrophic failure occurs and then to operate the circuits below that point, the sequence for this test is as follows:

a. Operate four circuits for 16 hours at +65°C. Monitor the outputs for functionality and record the power supply current at the start and end of test.

b. Perform interim electrical tests at +25°C.

c. Increase the operating temperature in 10°C increments until malfunction or permanent parameter shift occurs.

From the data obtained, two temperatures were selected and the life test started.

5. High Temperature Life Test

The parts were divided into two groups and the life test run. Two devices had been held out from the beginning as control devices. The supply voltages and each of the device outputs were monitored on a daily basis.

Interim electrical measurements were taken at 4, 8, 16, 32, 64, 128, 256, 500, 1,000 and 2,000 hours cumulative. Following 4,000 hours full electrical testing was performed. Failures were removed as they occurred and analyzed. The Reticon devices were run at 170°C and 185°C. The Fairchild devices were run at 150°C and 200°C. The Reticon life test was performed first followed by the Fairchild life test.

6. Temperature Cycle

Six devices were subjected to 1,000 temperature cycles from 150°C to -65°C per MIL-STD-883, Method 1010. Two devices were taken from each of the life test groups and two devices had not been through the 4,000 hour life test. Interim electricals were taken at 20, 50 250, 500, and 1,000 cycles.

7. Overvoltage Tests

Numerous pin combinations were stressed to breakdown to determine the weaknesses on the chip. Following breakdown, the test was repeated to determine whether a gate oxide failed or the input diode had gone into breakdown. The outputs were each shorted to ground to simulate output short circuit conditions. After failure had been induced, the devices were examined to analyze the failure sites.

8. Failure Analysis

All units which failed during the testing were reviewed for failure analysis. These were grouped by failure mode and typical samples of each type analyzed.

The analyses performed were of sufficient detail to determine the failure mode, failure mechanism, probable cause, and the relationship between the failure and the conditions at the time of failure.

9. Data Analysis

The data taken during this testing was stored on cassette tape and also on computer printout. Analysis was made during the testing to determine any trends in the parametric changes. Following the life tests end-to-end evaluations were performed. Further data analysis was performed as indicated by the above.

III. Introduction to CCDs

A. CCD Principles

The invention of the charge-coupled device was announced by Bell Laboratories in March of 1970. There has been a significant amount of research on this unique device in the past ten years.

The CCD shift register is basically an array of closely spaced MOS capacitors. The voltage on these capacitors, or electrodes, produces an inversion layer within the silicon which is capable of holding charge. By changing the voltage levels applied to these electrodes in a systematic manner, the charge can be transported along the CCD.

There are many practical ways to construct a device so that it will transfer a charge packet from input to output. These devices have at times been referred to as Charge Transfer Devices (CTD's). They include the Charge Coupled Devices (CCDs) and the Bucket Brigade Devices (BBD's). Because of the apparent electrical superiority and higher packing density of the CCDs these were selected for study.

There are two basic types of CCDs. These are surface-channel devices (SCCD) and buried-channel devices (BCCD). The difference in physical construction between these two technologies is an additional diffusion for the BCCD. There is a layer of material, next to the surface, that is of opposite doping to the substrate.

In addition to the two different types of channels utilized in CCDs there are many variations in the clocking modes utilized. There are two-phase, three-phase, and four-phase clocking schemes. There are also several types of electrodes utilized including single level aluminum, single level doped polysilicon, aluminum and polysilicon gates, two levels of polysilicon, and three levels of polysilicon. Some of these variations will be discussed in this section.

B. Surface Channel CCD

The surface channel device is illustrated in the cross-section in Figure III-1A. The energy band diagram with a positive bias applied to the gate is shown in Figure III-1b, and with charge present in Figure III-1c. It is evident that the charge resides at the $Si-SiO_2$ interface. This is the origin of the term surface channel. When the clock pulses the electrode the silicon beneath this area is driven into deep-depletion. Charge can be stored in this region for a time much shorter than the thermal relaxation time of the capacitors. The CCD is therefore a dynamic device.

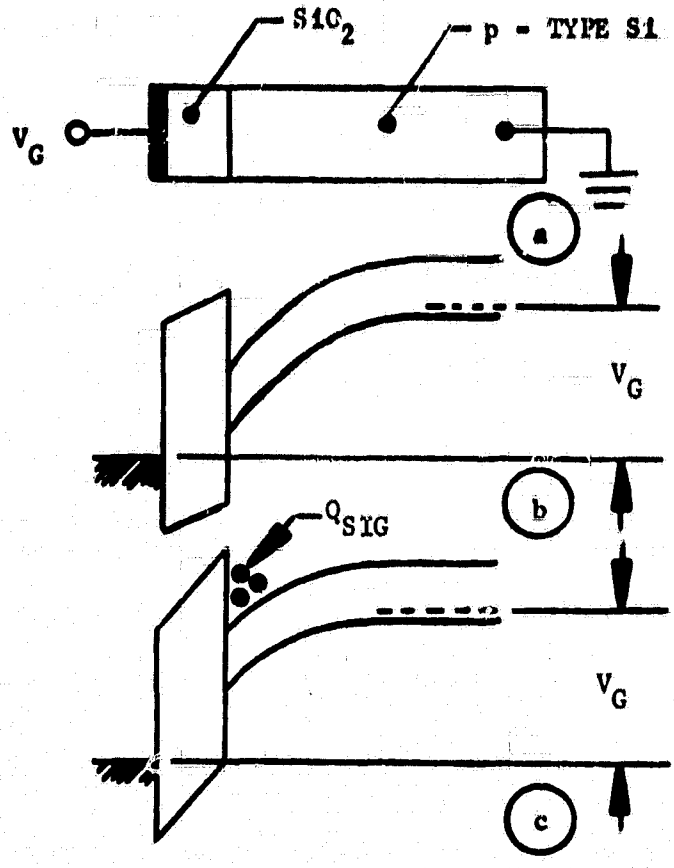


Figure III-1 Surface Channel CCD:

a) Cross Section

b) Energy Band Diagram with Positive Gate Bias

c) Energy Band Diagram with Charge Present

A three-phase clocking scheme is shown in Figure III-2. This diagram has every third electrode connected to the same clock. The charge resides beneath the electrode that is at a positive potential. At time T1 the charge resides beneath the $\phi 1$ electrode. At time T2 the charge is being transferred to the area beneath the $\phi 2$ electrode. The $\phi 1$ clock is going low and the $\phi 2$ clock is high. At time T3 the charge is being transferred to the area beneath the $\phi 3$ electrode.

This process continues and the charge is transferred along the shift register. A very similar clocking method can be used for a four-phase system. This system has one additional clock which is connected to every fourth electrode.

A two-phase system requires an additional element to produce directionality for the charge transport. The connections for a two phase system are shown in Figure III-3. Two adjacent gates are connected to the same potential, however, a different well potential is produced beneath them. This can occur due to a difference in the thickness of the insulator beneath the adjacent electrodes or due to a difference in the work function of the electrodes. Ion-implanted barriers along the channel have also been utilized on two-phase CCDs. In Figure III-3 the difference in the depth of the wells is due to a work function difference between the cross-hatched gates and the gates with diagonal lines. The clock signals are as shown. With $\phi 2$ high the charge will reside beneath these electrodes. When $\phi 1$ goes high and $\phi 2$ goes low the charge will be transferred to the right. A variation on the two phase clocking is to leave one voltage fixed at an intermediate level and clock the second as previously shown. This will allow the charge to move along the channel and will be discussed in more detail for the CCD321A-2.

C. Buried Channel CCD

The physics of operation of a BCCD are somewhat more complicated than that of an SCCD. The operation of a surface-channel CCD is closely related to the characteristics on an MOS capacitor in deep depletion. The operation of a buried-channel CCD is related to the characteristics of a depletion-mode MOS capacitor in punch-through state. In this situation the gate is over an n-type material which has been reverse biased with respect to the substrate. The punch-through condition occurs when the depletion region created by the reverse biased p-n junction merges with that beneath the gate.

An energy band diagram for a BCCD is shown in Figure III-4. Figure III-4a shows the cross-section. Figure III-4b shows the energy band diagram with a positive gate bias. Figure III-4c shows the band bending which occurs when charge is stored. The area shown by X_{CH} is the area where charge resides. As is visible, the charge is removed from the $Si-SiO_2$ interface and losses due to interaction with the surface are eliminated. If an excessive amount of charge is stored, X_{CH} will reach the surface and losses will occur.

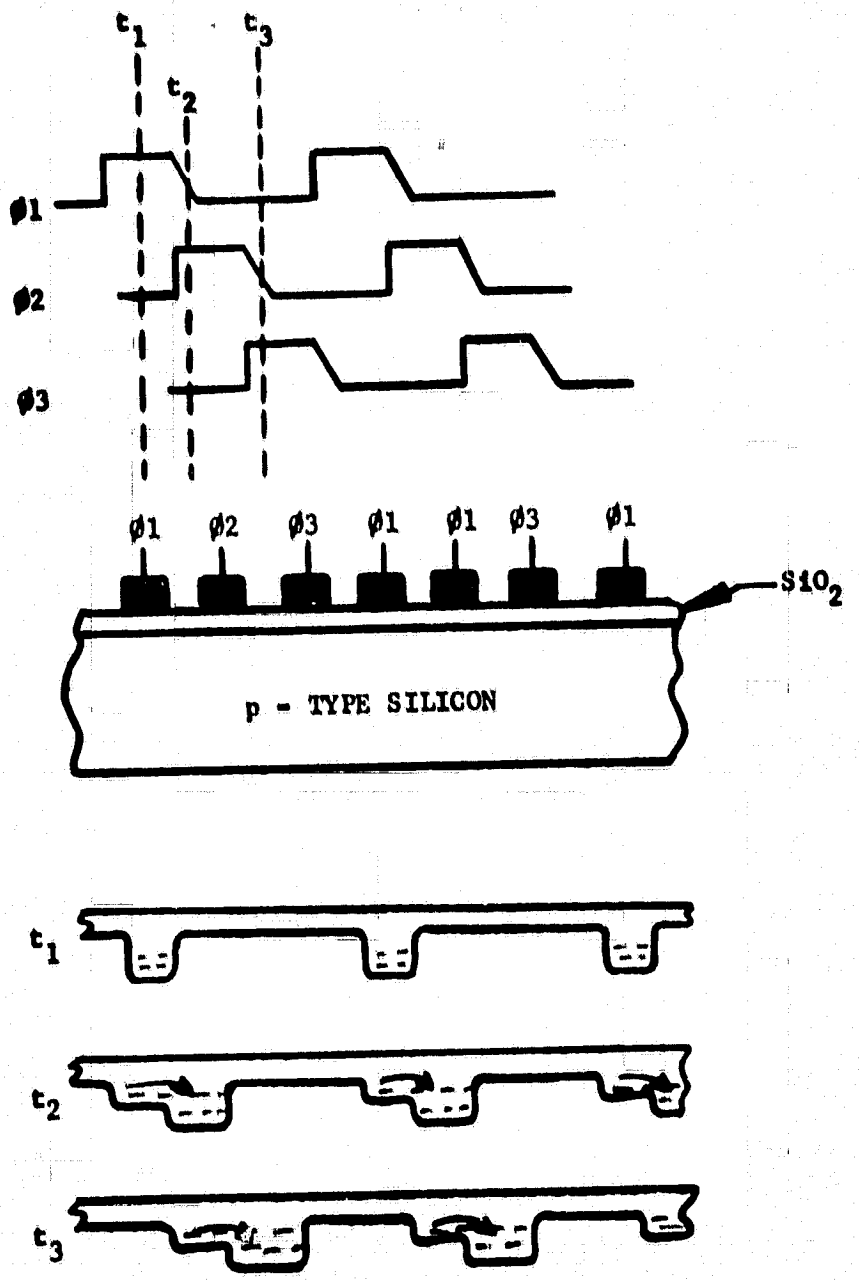


Figure III-2 Surface Channel CCD with Three Phase Clocking Scheme

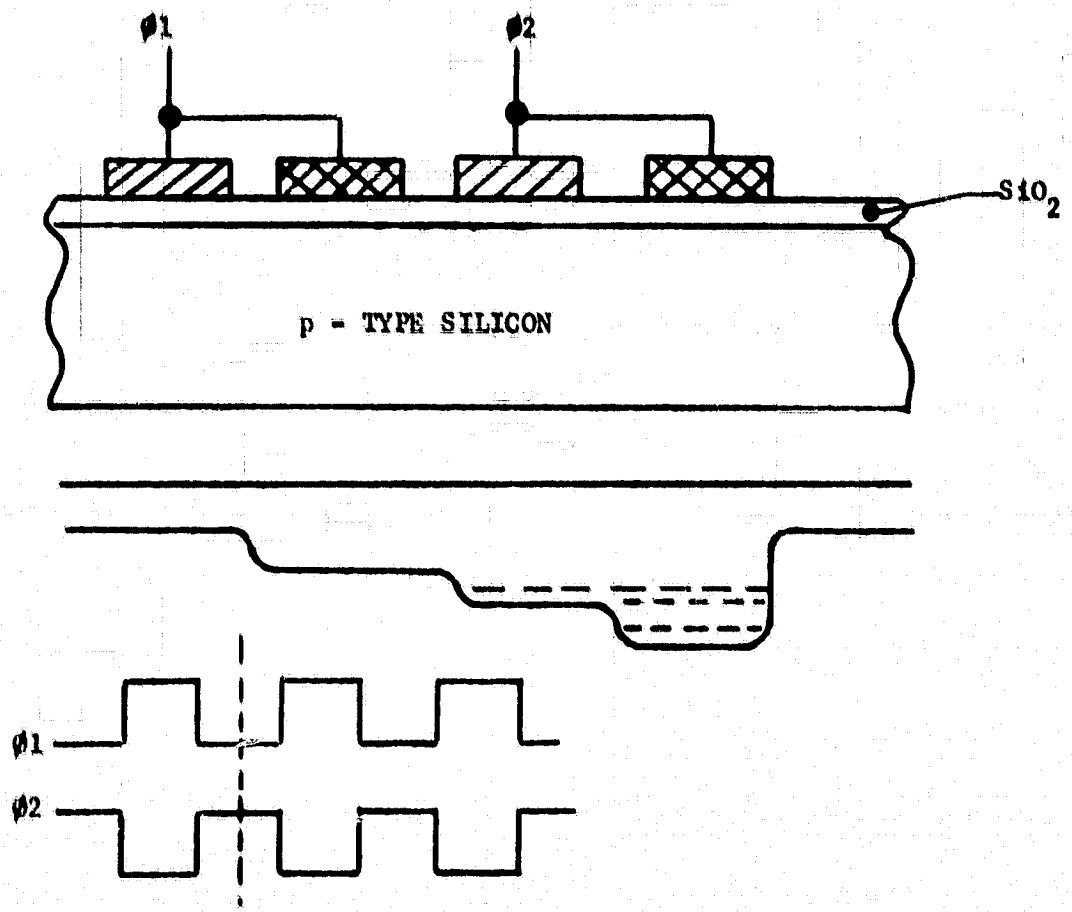


Figure III-3 Surface Channel CCD with Two Phase Clocking Scheme

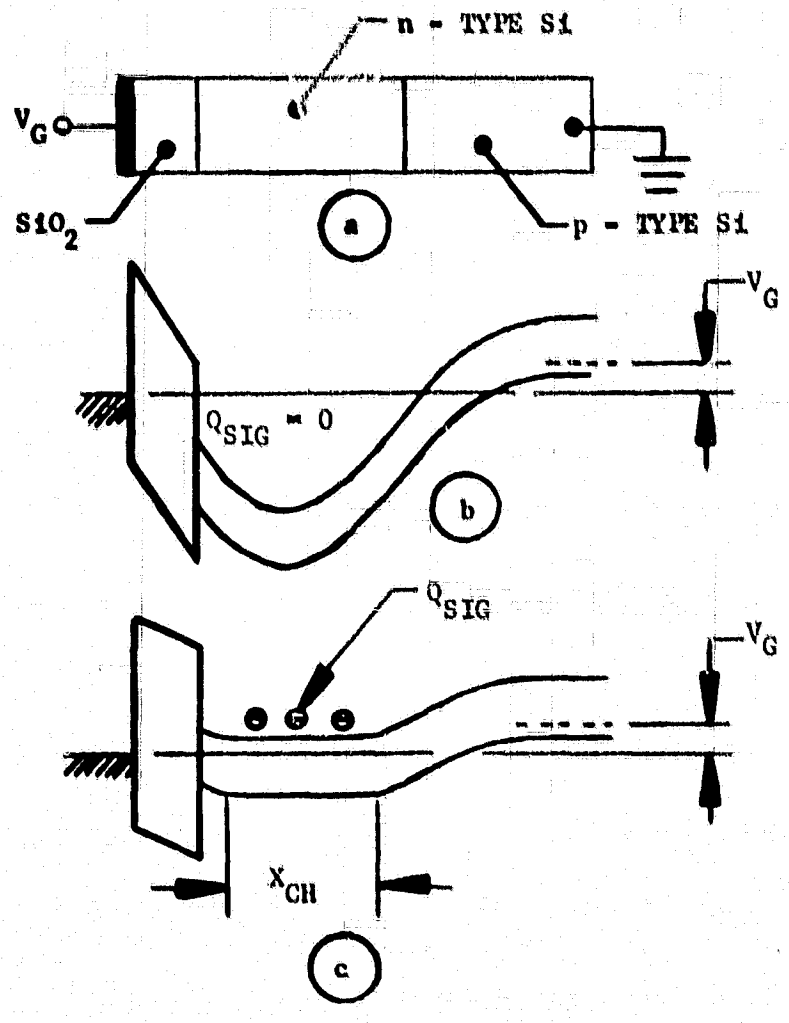


Figure III-4 Buried Channel CCD:

a) Cross Section

b) Energy Band Diagram with Positive Gate Bias

c) Energy Band Diagram with Charge Present

A cross-section of a BCCD is shown in Figure III-5. The input and output diodes are reverse biased to deplete the n-layer. The gates again are coded as in Figure III-3, with the cross-hatched gates having the lower flatband voltage. At time t1 the high voltage on ϕ1 will produce a large area in which charge can reside beneath it. The low voltage on ϕ2 will pinch-off the channel beneath it. The equipotential field lines within the n-layer will appear approximately as shown by the dotted lines in Figure III-5. The charge will move down the channel in a manner that has been compared to the peristaltic process of moving something down an enclosed canal in wavelike constrictions.

D. Comparison of Surface and Buried Channel CCDs

The transfer efficiency of the BCCD is higher than the SCCD. This is related to strong fringing fields and also to an improvement in mobility due to charge transfer within the bulk rather than at the surface. Charge transfer mechanisms include drift due to self-induced fields, fringing fields, and thermal diffusion. The fringing field magnitude is very difficult to calculate, however, it increases for thicker oxides, greater clock swings and smaller electrode lengths. The channel on the BCCD is separated from the gate electrode by a greater distance due to the fact that it is buried beneath the surface. This creates the higher fringing fields. The fringing field is a very important factor for the transfer of the last 1% of charge between adjacent electrodes. The self-induced fields are more important for the majority of the charge transfer.

The operating frequency of the BCCD is also higher. This is again related to the fringing fields and bulk mobility. 100 MHz clock frequencies are possible with the BCCD.

The BCCD has smaller charge handling capabilities than the SCCD. This is on the order of one third. The BCCD can however transport a smaller charge packet so its dynamic range may be wider.

The BCCD can have a higher dark current because of large thermal generation by the empty surface states. This can limit the operating temperature range.

By eliminating the interactions of the signal charge with the surface states the noise in the buried channel device is very low.

E. Applications

There are three categories of applications for CCDs. These are Image Sensors, Digital Memories and Analog Signal Processors.

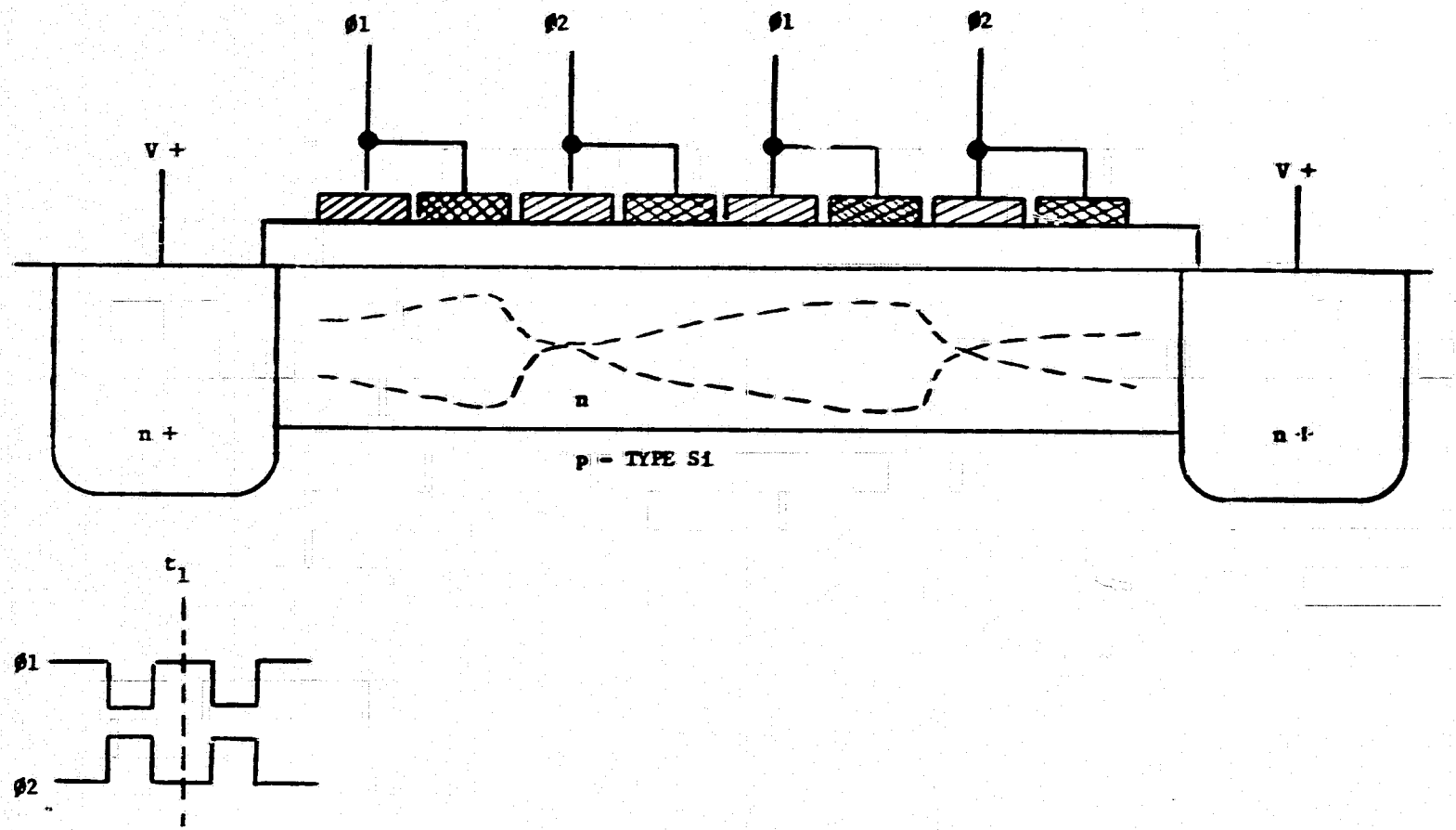


Figure III-5 Buried Channel CCD Cross Section with Equipotential Field Lines

The Image Sensors take a variation in the light intensity which reaches the sensor elements, transfers this through a shift register, and produces an electrical output which provides spatial resolution of the image on the sensors (e.g., TV camera). These chips are constructed as either a long single line of sensors or as an area array.

The CCD is used in Digital Memory applications as a dymanic serial type memory. They require periodic refresh because of the physics of their operation and they are basically shift register in nature which makes them serial rather than random access. They find applications in such things as cache memory and bulk storage. They are high density devices with low power consumption.

The area of interest for this study are the CCDs used as analog shift registers. These shift registers are of various lengths and can be operated over a range of frequencies. Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverbration effects in stereo equipment, and voice scrambling.

IV Reticon R5101

A. Physical Construction

The R5101 is a surface channel CCD. The following section will discuss its' construction. This will include physical dimensions and type of package, residual gas-analysis, circuit schematics, microsections, and examination of the individual layers. Reliability considerations relative to these areas will be discussed.

1. Package

The R5101 is in a 22 pin ceramic dual-in-line package (Figure IV-1). This is a multilayer side braze construction with a braze sealed metal lid. Pin 1 is marked by a dot on the top of the ceramic. The metal lid on this package type is normally electrically connected to Pin 1, however, this was mechanically opened by the manufacturer on this part type. There are 11 leads on each side of this package at 0.1 inch spacings. The package width is 0.4 inches. The serial number was placed on the package to keep device identity during the course of the testing.

2. Residual Gas Analysis

The long-term reliability of a device is affected by the internal package ambient. This ambient was measured using a CEC Mass Spectrometer Model Number 21-614 with a specially designed inlet system. This inlet system was designed to optimize the detection of the moisture within the devices being tested. The volume of the puncture tool and inlet line are kept to a minimum so that packages with small internal volumes can be analyzed. The Reticon package had a volume of 0.1cc and created a pressure rise of 500 microns within the puncture tool. This is an adequate quantity of gas to perform an analysis. The puncture tool with the device in place is heated to approximately 110^{o}C and kept at this temperature for a minimum of 16 hours. The inlet line from there to the analyzer is kept at an elevated temperature slightly higher than that of the puncture tool. The gold leak immediately before tha analyzer is at a vacuum level of 10^{-6} Torr during this bakeout. This high temperature bake releases moisture trapped in the inlet as well as preparing the samples for analysis.

Following the 16 hour bake a background run is performed and recorded. This is used to substract the background gases from the package gases following the package RGA run. The puncture tool area is isolated and the pressure inside that chamber is monitored while a hole is made in the device lid with a puncture tool. When a pressure rise is indicated the device

Figure IV-1 Overall View of Reticon R5101 Package; X4.

has been punctured and the analysis can begin. A portion of the gas is released into the inlet system to obtain approximately a 100 micron pressure rise. The RGA is then performed and recorded. The table below lists the gases detected and their mole percentages.

GAS	S/N35	S/N 0
Nitrogen N_2	99.12	99.03
Oxygen O_2	.16	.50
Water H_2O	<.01	<.01
Carbon Dioxide CO_2	.54	.34
Methane CH_4	<.01	.02
Argon Ar	.16	.09

This is an acceptable gas ambient and does not represent a reliability concern for this device.

3. Capacitance Versus Voltage Plots

C-V curves taken on an MOS structure can provide information on the presence of mobile ionic contamination within the thermal oxide. This characteristic was measured on two R5101 devices. It was measured on V_{IG} and V_{OG} on serial number 4 and on V_{OG} on serial number 3. These measurements required mechanical isolation and probing of the die surfaces V_{IG} was accidentally damaged on S/N 3 and could not be measured.

The input protect circuitry on the pins made it necessary to isolate it from the gate area to obtain capacitance measurements for both a positive and negative gate bias. The procedure used for these circuits was to bias the part to 15 volts with the gate of interest positive with respect to the substrate. This was then placed in an oven for 10 minutes at 300 °C. The bias was maintained on the device after removal from the oven until the part was cooled down. This will tend to drive the positive ions away from the postively biased gate toward the $Si-SiO_2$ interface. These ions will then exert a larger influence on the semiconductor and cause a shift in the C-V curve. Since these are positive ions, the C-V curve will shift toward a more negative gate potential. The voltage level on the gate that is necessary to overcome the charge in the oxide is the flatband voltage (V_{FB}). This voltage is equal to:

$$V_{FB} = \phi ms - \frac{Qss}{Co}$$

ϕ_{ms} = Work function difference between the gate and the silicon.

Q_{ss} = Fixed surface - state charge density per unit area.

C_o = Oxide capacitance per unit area.

For a given gate, ϕ_{ms} and C_o will stay constant so that a change in the flatband voltage level will be equal to:

$$\Delta V_{FB} = \frac{\Delta Q_{ss}}{\Delta C_o}$$

A change in Q_{ss} then indicates a movement of charge to the SiO_2-Si interface. This charge will be termed Q_o, the mobile ion impurity concentration per unit area. Therefore:

$$\Delta V_{FB} = \frac{Q_o}{C_o}$$

For a given gate oxide thickness this can be converted to Q_o/q.

$$\Delta V_{FB} = \frac{Q_o}{C_o}$$

$$Q_o = \Delta V_{FB}\, C_o$$

$$\frac{Q_o}{q} = \frac{\Delta V_{FB}\, C_o}{q}$$

where $C_o = \frac{K_o\, \epsilon_o}{X_o}$

and K_o = dielectric constant of SiO_2 = 3.9

ϵ_o = permittivity of free space = 8.86×10^{-14} F/CM

X_o = oxide thickness

q = magnitude of electronic charge = 1.6×10^{-19} Coulombs

With the moblie ions now residing at the $Si-SiO_2$ interface, the part was mechanically opened and the aluminum metallization between the gates and the input protect circuit was scribed open. The measurements were then taken between V_{IG} and the channel input diode and between V_{OG} and the common n+ diffusion of Q2, Q4, and Q6 gate. These measurements were taken using the mechanical probing station and are recorded in Table IV-1. These readings are taken with the DC bias as shown in the Figure. A 50 mV AC signal at 1 MHz is superimposed on this DC bias. The capacitance readings and the normalized readings are given in this table. The parts were then baked at 300°C for 10 minutes to redistribute the mobile charge and the parts were remeasured. These are again listed in Table IV-1. The plots of these normalized values are given in Figure IV-2. The dots are the readings following bias and the X's are the readings following anneal. There is no apparent shift between these curves indicating a clean oxide process.

4. Schematic

The R5101 is a 2000-sample analog delay line. It is on a single chip with a self-contained four-phase clock generator-driver and input and output circuitry. A functional schematic from the Reticon data sheet is redrawn in Figure IV-3. This shows the two MOS devices associated with the input signal, a representation of the channel which is overlapped by gates that are tied back to the clock and driver circuitry and it shows the single channel splitting into two separate channels feeding into the output circuitry. The sections will be covered in detail and their physical location and structure discussed. An overall die photograph is shown in Figure IV-4. The clock circuitry along the bottom edge generates the four phases used on this device. The input circuitry is in the lower right hand corner at the start of the channel. The channel winds back and forth until it reaches the output circuitry in the upper left hand corner.

a. Clock Circuitry - The clock circuitry is shown in Figure IV-5. This shows the clock generator and the four driver circuits. The sync and clock inputs are labeled. These clocks go through an input protect circuit and then to the clock generator. Figure IV-6 shows a higher magnification photograph of the clock generator circuitry. The individual transistors are labeled. The schematic for this is shown in Figure IV-7, the logic diagram in Figure IV-8, and the timing diagram is shown in Figure IV-9. All of the transistors on this device are n-channel enhancement mode silicon gate field effect transistors.

TABLE IV-1a C-V PLOT DATA, V_{OG}, S/N 3, R510J

DC Bias	15 V for 10 min. at 300°C		Annealed	
	Capacitance (0.01 pf)	Normalized	Capacitance (0.01 pf)	Normalized
-4	21.0	.664	19.4	.660
-3	21.4	.677	19.7	.670
-2	22.4	.709	20.6	.701
-1	24.4	.772	22.4	.762
-0.5	25.6	.810	23.9	.813
-0.1	27.2	.861	25.2	.857
0	28.3	.896	26.4	.898
0.5	29.5	.934	27.2	.925
1	31.6	1.0	29.4	1.0
1.5	31.4	.994	29.4	1.0
2	31.2	.987	28.2	.960
3	29.8	.943	27.6	.939
4	29.4	.930	26.8	.912
5	28.8	.911	25.8	.878

TABLE IV-1b C-V PLOT DATA, S/N 4; R5101

VOG					VIG				
10 MIN 300°C 15 V			ANNEALED		10 MIN 300°C 15 V			ANNEALED	
CAPAC X 0.01 uF	NORMAL-IZED	DC BIAS	CAPAC X 0.01 uF	NORMAL-IZED	CAPAC X 0.01 uF	NORMAL-IZED	DC BIAS	CAPAC X 0.01 uF	NORMAL-IZED
19.8	.627	-4	20.8	636	343.0	1.0	-4	340.4	1.0
20.6	652	-3	21.4	654	343.0	1.0	-3	340.0	.999
21.6	684	-2	22.4	685	343.0	1.0	-2	339.7	998
23.3	737	-1	24.0	734	342.6	999	-1	339.4	997
25.0	791	-0.5	25.8	789	342.2	998	-0.5	338.8	995
26.2	829	-0.1	27.6	844	342.2	945	-0.1	321.4	944
27.0	854	0.1	28.2	862	310.8	906	0.1	307.0	902
28.0	886	0.5	29.6	905	296.2	864	0.5	292.6	860
30.6	968	0.8	31.8	972	289.4	844	0.8	284.6	837
31.6	1.0	1	32.7	1.0	286.2	834	1	282.0	828
31.2	987	2	32.2	985	275.4	803	2	271.6	798
30.6	968	3	31.7	969	269.4	785	3	264.6	777
30.2	956	4	31.4	960	265.2	773	4	260.6	766
29.8	943	5	30.8	942	262.0	764	5	258.3	759
					259.8	751	6	255.2	750

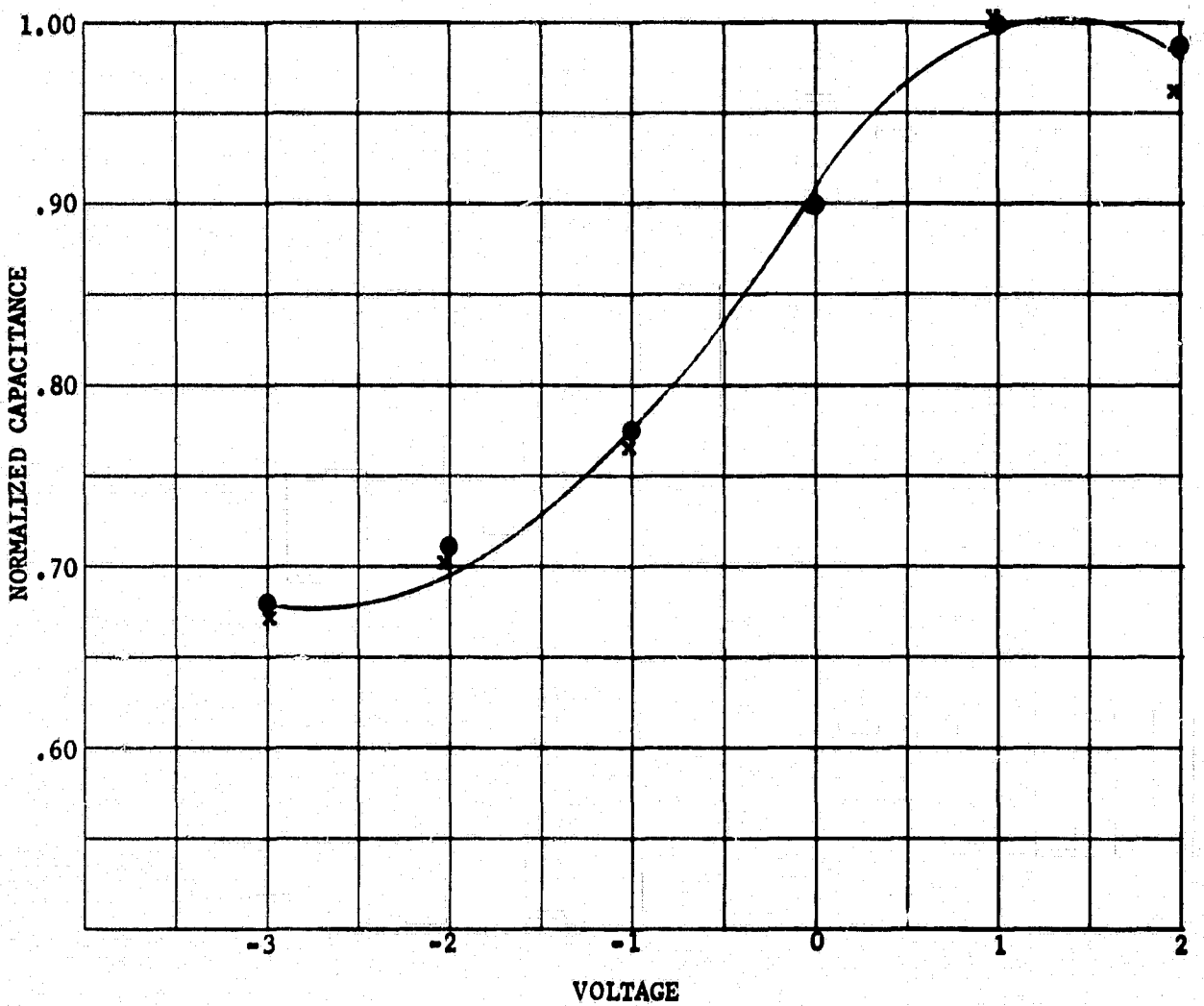


Figure IV-2a V_{OG}, S/N 3; R5101

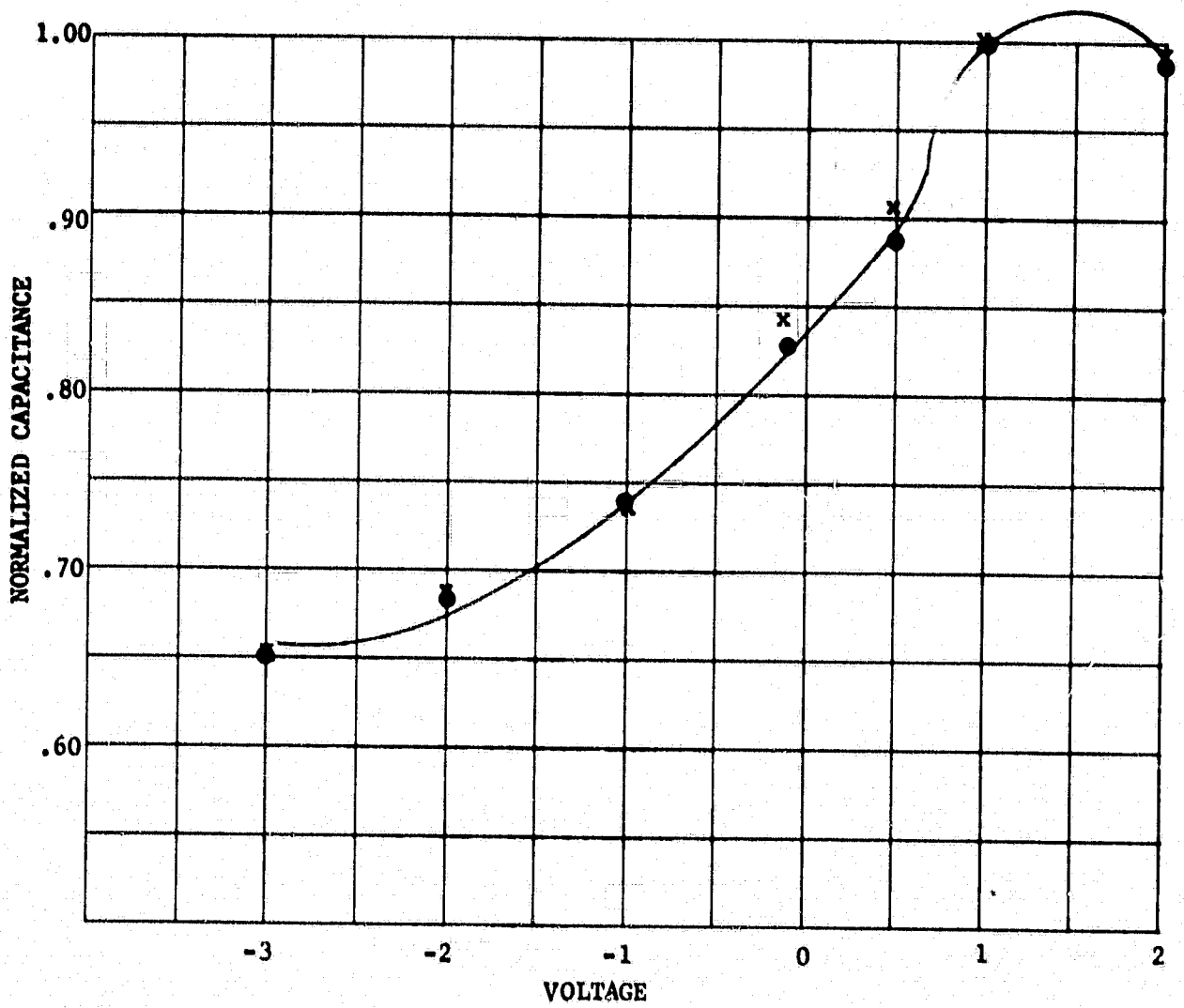


Figure IV-2b V_{OG}, S/N 4; R5101

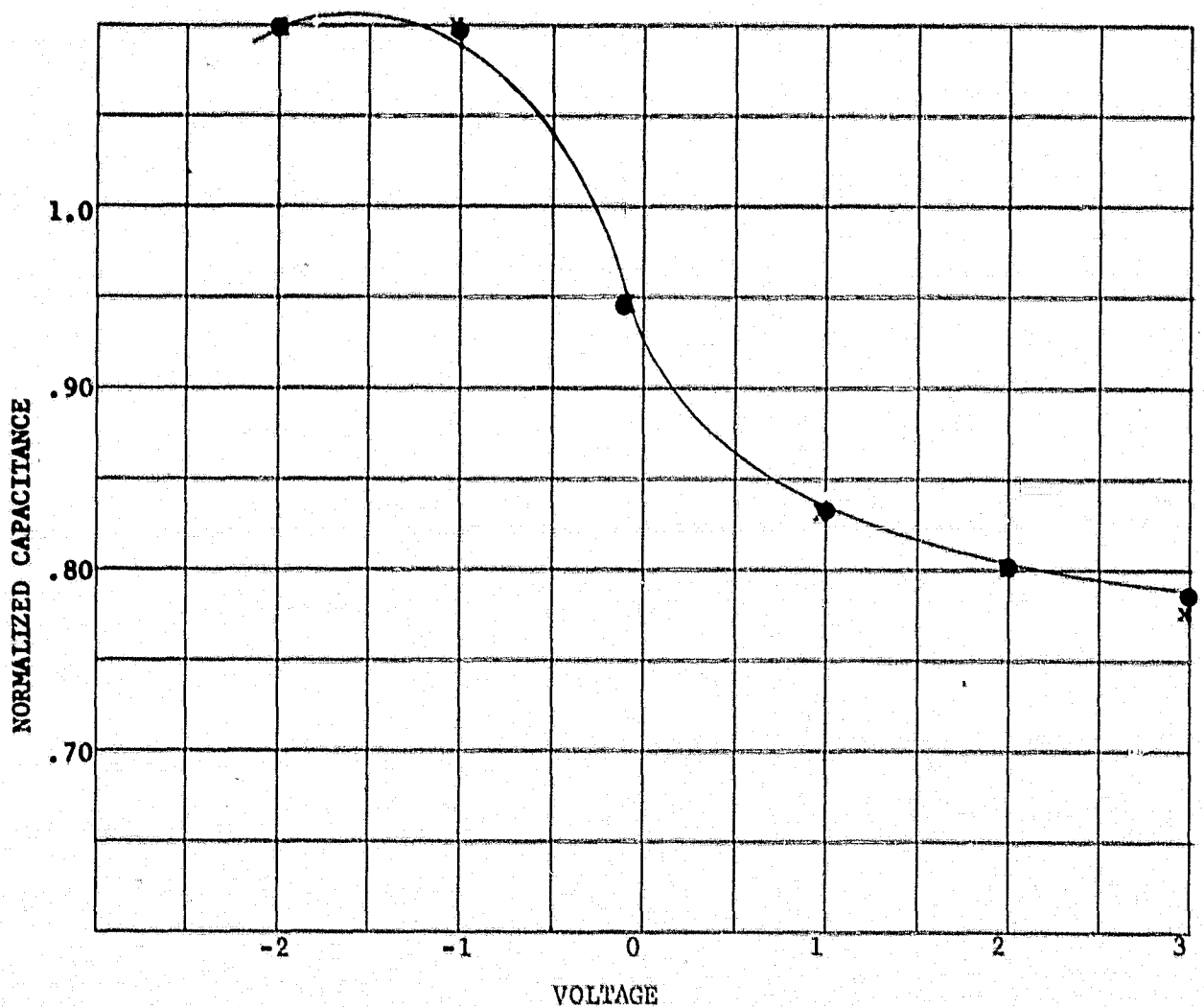


Figure IV-2c V_{IG}, S/N 4; R5101

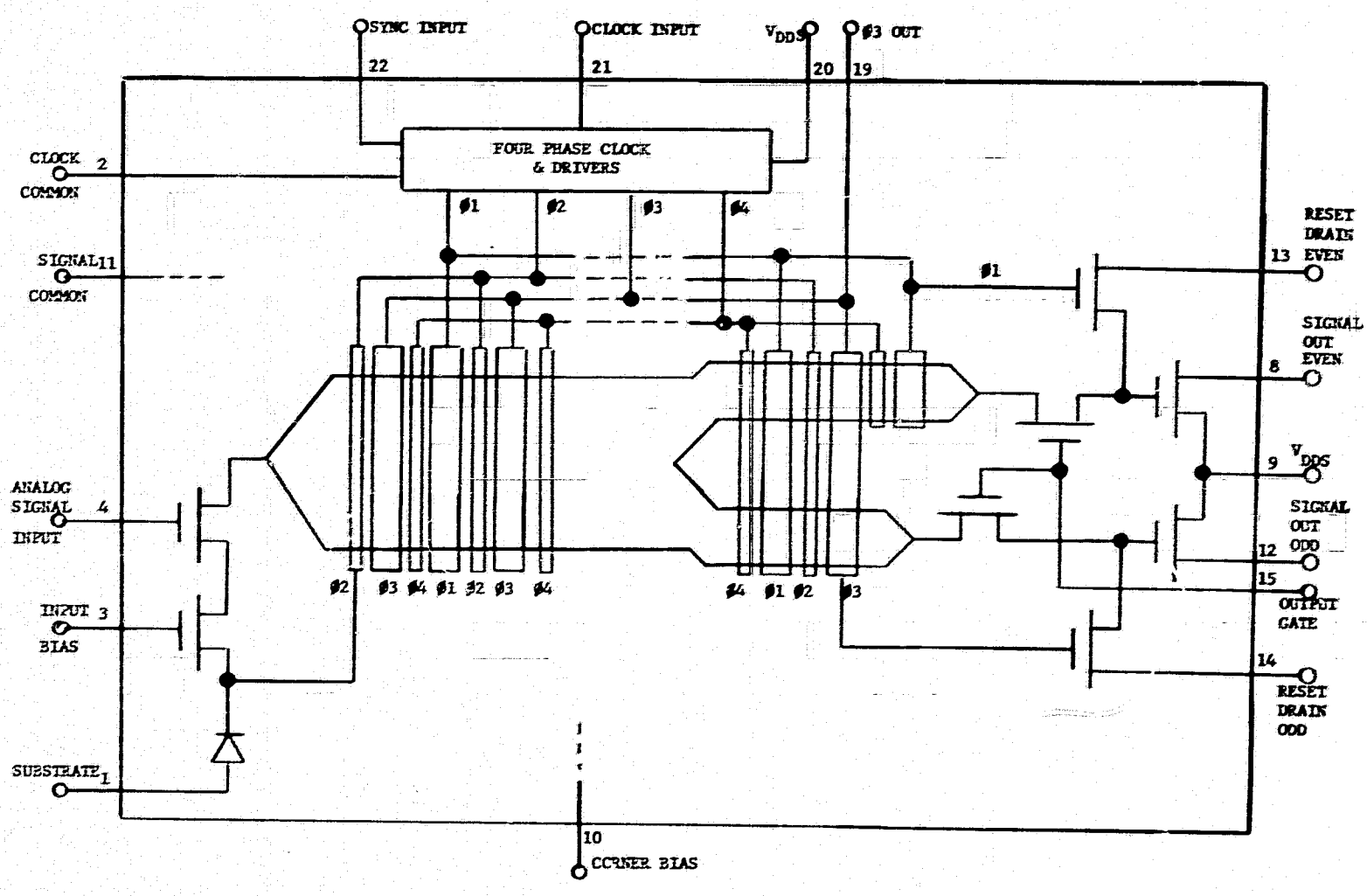


Figure IV-3 Functional Schematic, R5101

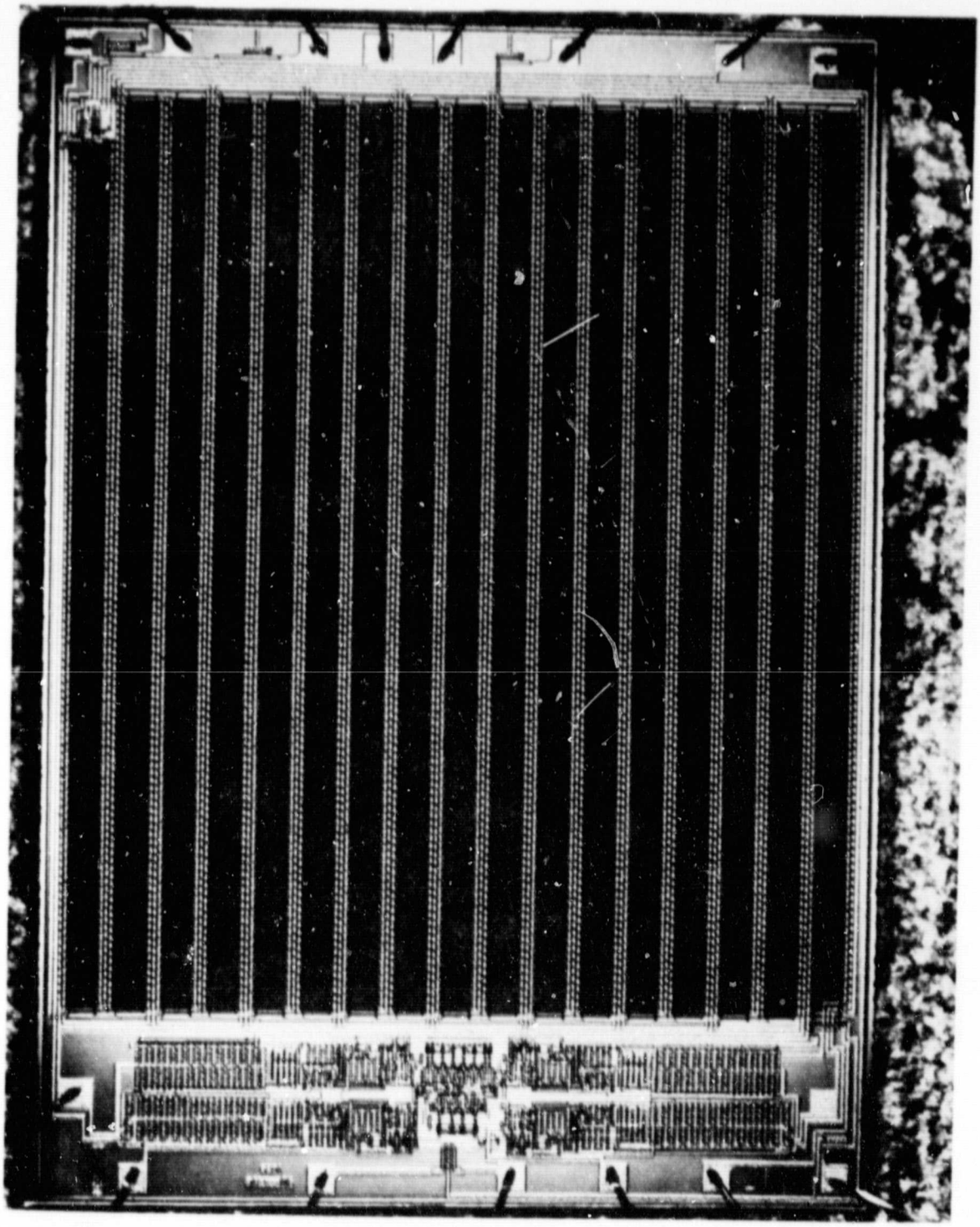


Figure IV-4 Overall Die Photograph, R5101; X40

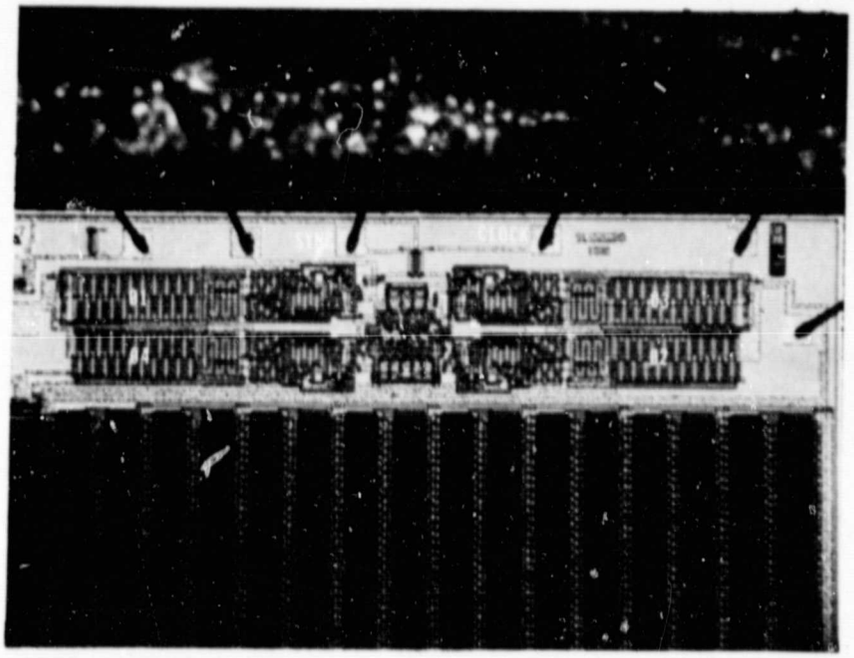


Figure IV-5 Clock Circuitry, R5101; X30

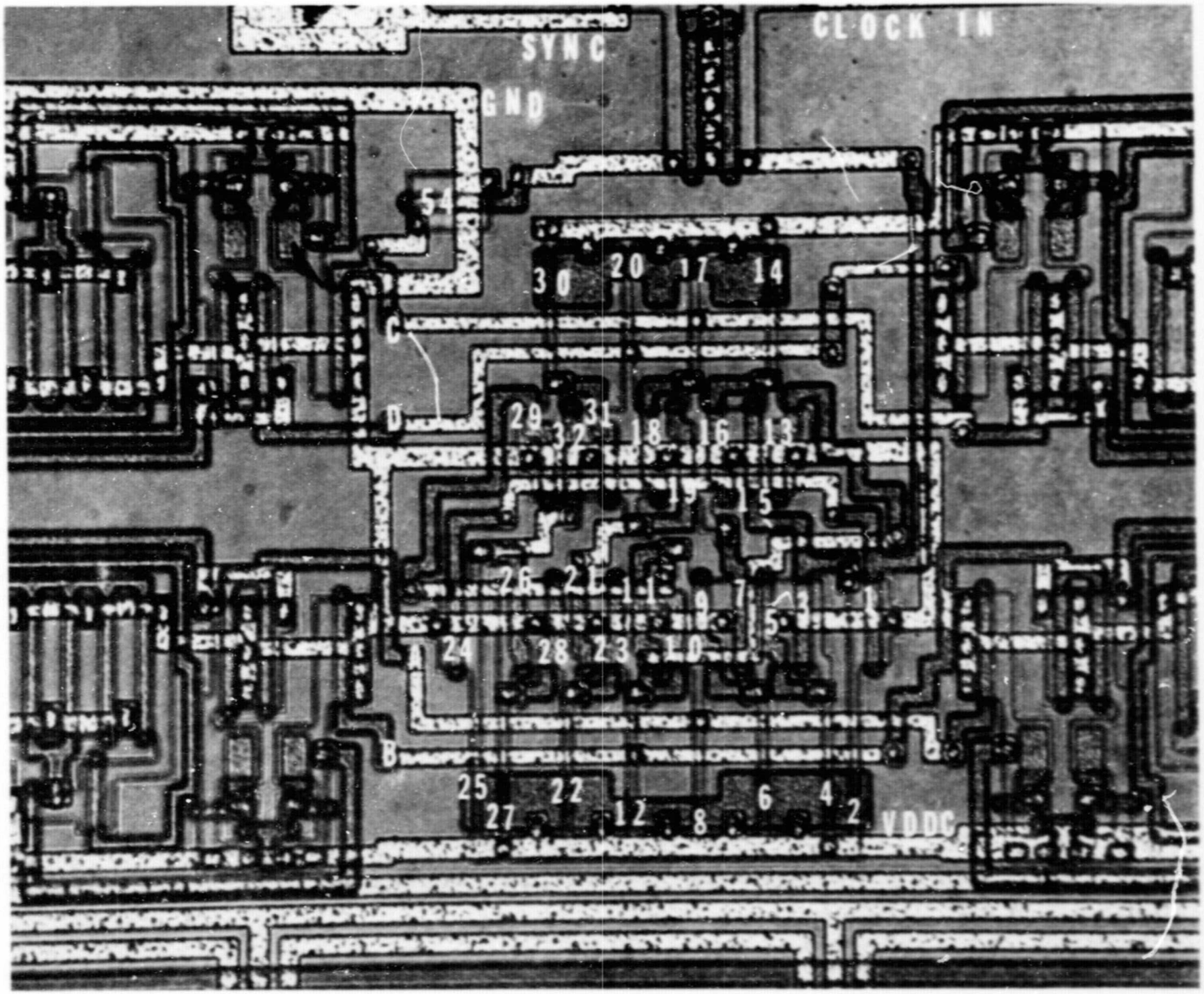


Figure IV-6 Clock Generator Photograph, R5101; X200

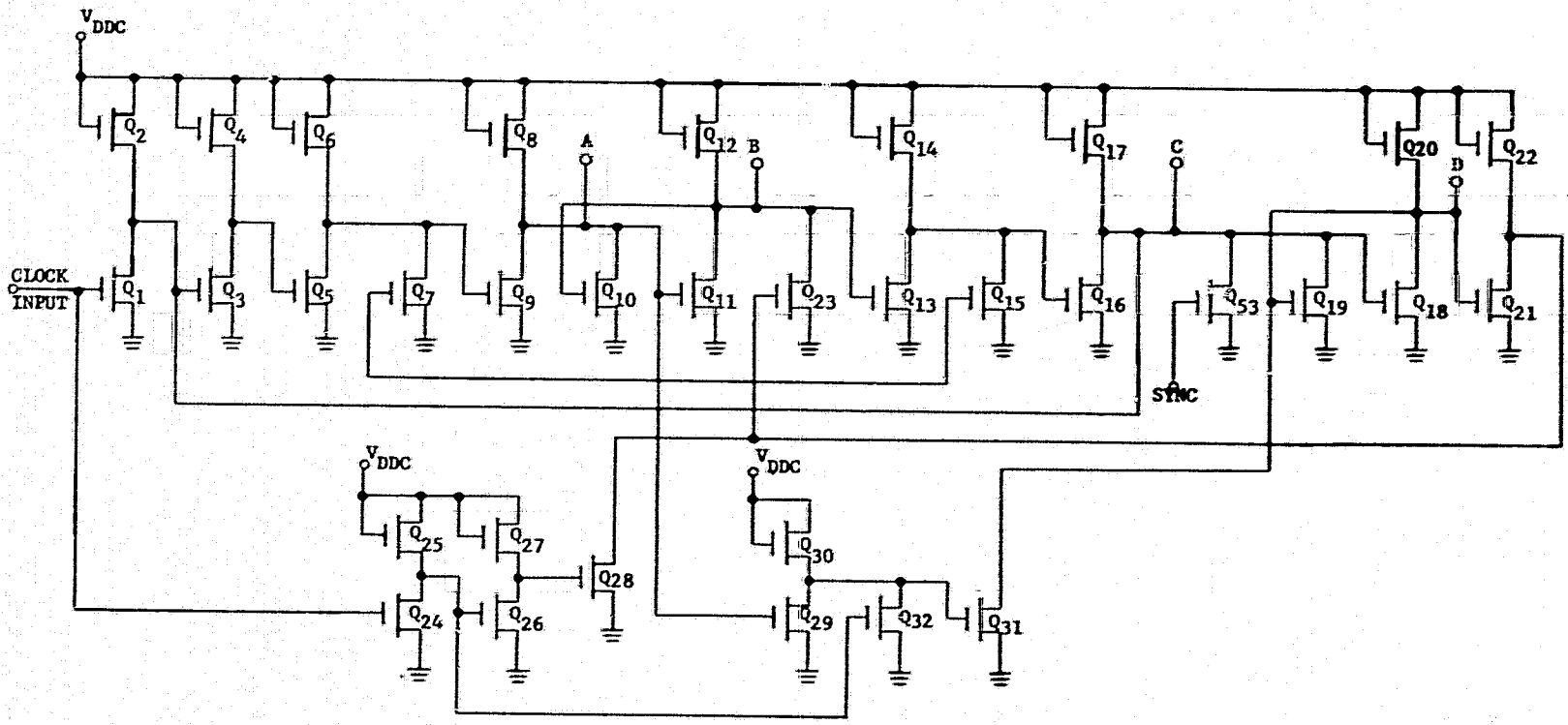


Figure IV-7 Schematic, Clock Generator, R5101

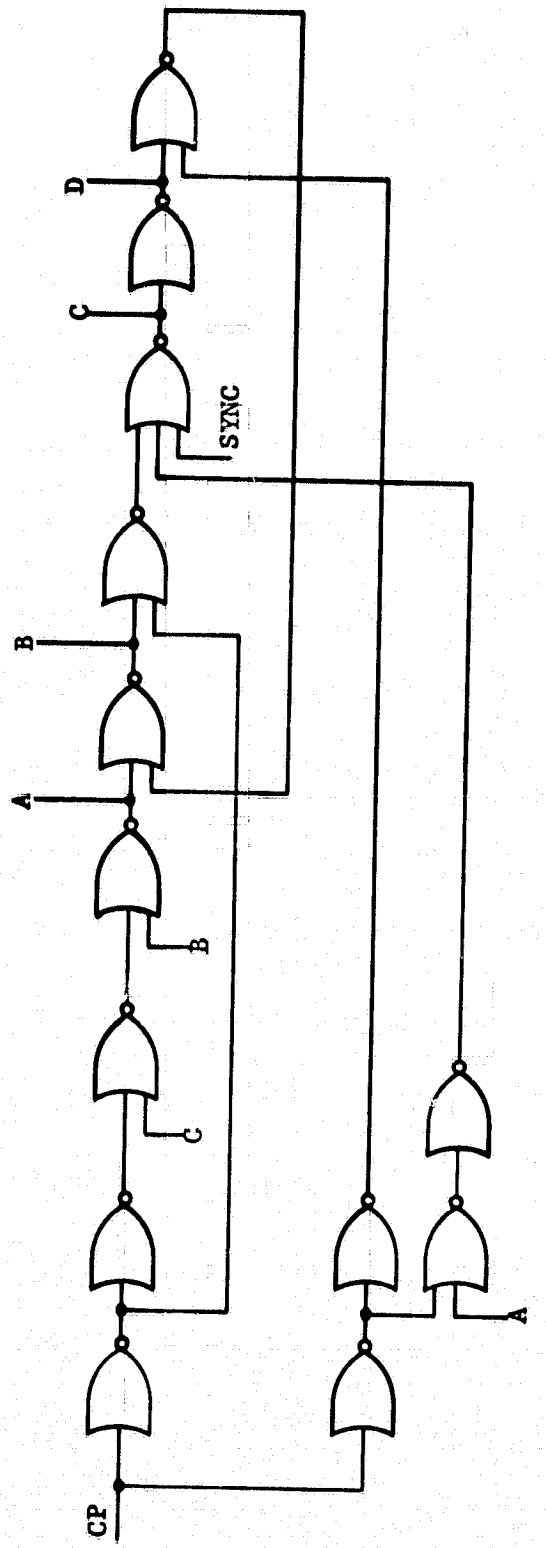


Figure IV-8 Logic Diagram, Clock Generator, R5101

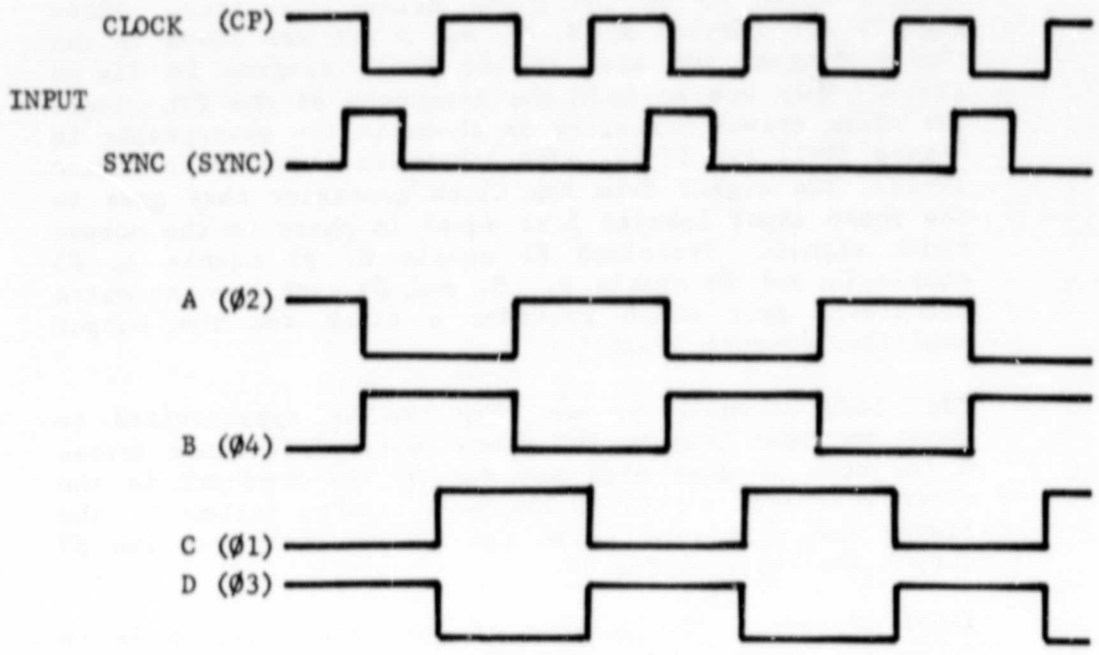


Figure IV-9 Clock Generator Timing, R5101

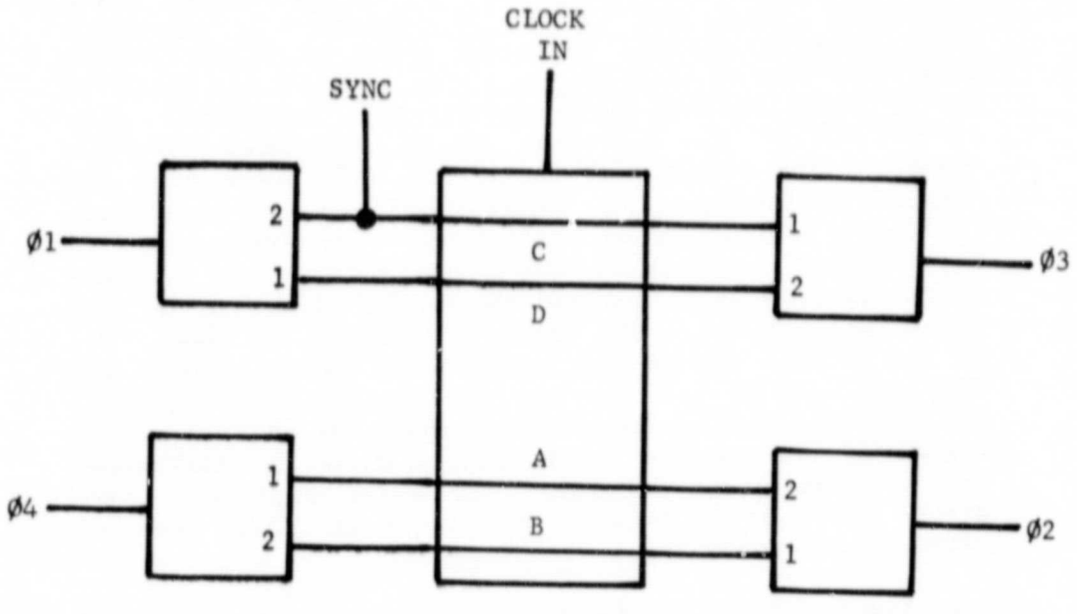


Figure IV-10 Block Diagram, Clock Generator, R5101

This circuit takes the TTL clock and produces four signals which go to the clock driver circuitry. These signals are labeled A, B, C, and D and are shown in the timing diagram and also in the block diagram in Figure IV-10. They are at half the frequency of the TTL clock. The clock driver circuitry is shown in the photographs in Figure IV-11 and IV-12. The schematic is shown in Figure IV-13. The signal from the clock generator that goes to the phase input labeled 2 is equal in phase to the output clock signal. Therefore $\phi 1$ equals C, $\phi 2$ equals A, $\phi 3$ equals D, and $\phi 4$ equals B. $\phi 1$ and $\phi 3$ each have an extra transistor pair which provides a clock for the output amplifier (Figure IV-14).

The clock circuits on one chip can be synchronized to those on other CCDs by the sync input. This input forces C low when it goes high and due to the feedback in the clock generator circuitry the other clocks follow C. The timing for this sync pulse can be obtained from the $\phi 3$ output available on Pin 19.

b. Input Circuit - The purpose of the input circuit is to introduce charge into the CCD channel. The amount of charge introduced is dependent upon the difference between V_{IG} and V_I. V_{IG} is the input bias gate voltage and is kept at a fixed potential, typically 3 volts. V_I is the analog signal input and this will vary from about 3 to 6 volts. The largest signal being introduced when V_I is at 6 volts. A schematic representation of this input is shown in Figure IV-15. This consists of a diode with the cathode connected to the $\phi 2$ clock and the anode connected to substrate. This is the source for electrons to be introduced into the channel. The transistors shown are only gates over the channel as indicated in Figure IV-16 and the photograph in Figure IV-17. These gates overlap as indicated. In the schematic the gates which are solid lines are the bottom layer polysilicon and the dashed lines are the top layer polysilicon. The gates connected to V_{DDC}, V_I, $\phi 3$ and $\phi 1$ are the bottom polysilicon layer (poly1) and V_{IG}, $\phi 1$, and $\phi 4$ are the top polysilicon layer (poly2). The vertical row of transistors shown in the schematic, Figure IV-15, are the input section while the horizontal row of transistors represent the shift register. From Figure IV-16 it is evident that there is little physical difference between these structures.

The input structure functions as indicated in Figure IV-16. At time T1 with $\phi 2$ low, electrons fill the potential wells created beneath the V_{DDC}, V_{IG} and V_I gates. At the end of this injection period, the surface potentials under these three gates will be the same as the input diode voltage. At time T2, $\phi 2$ goes high creating a depletion region and electrons are not

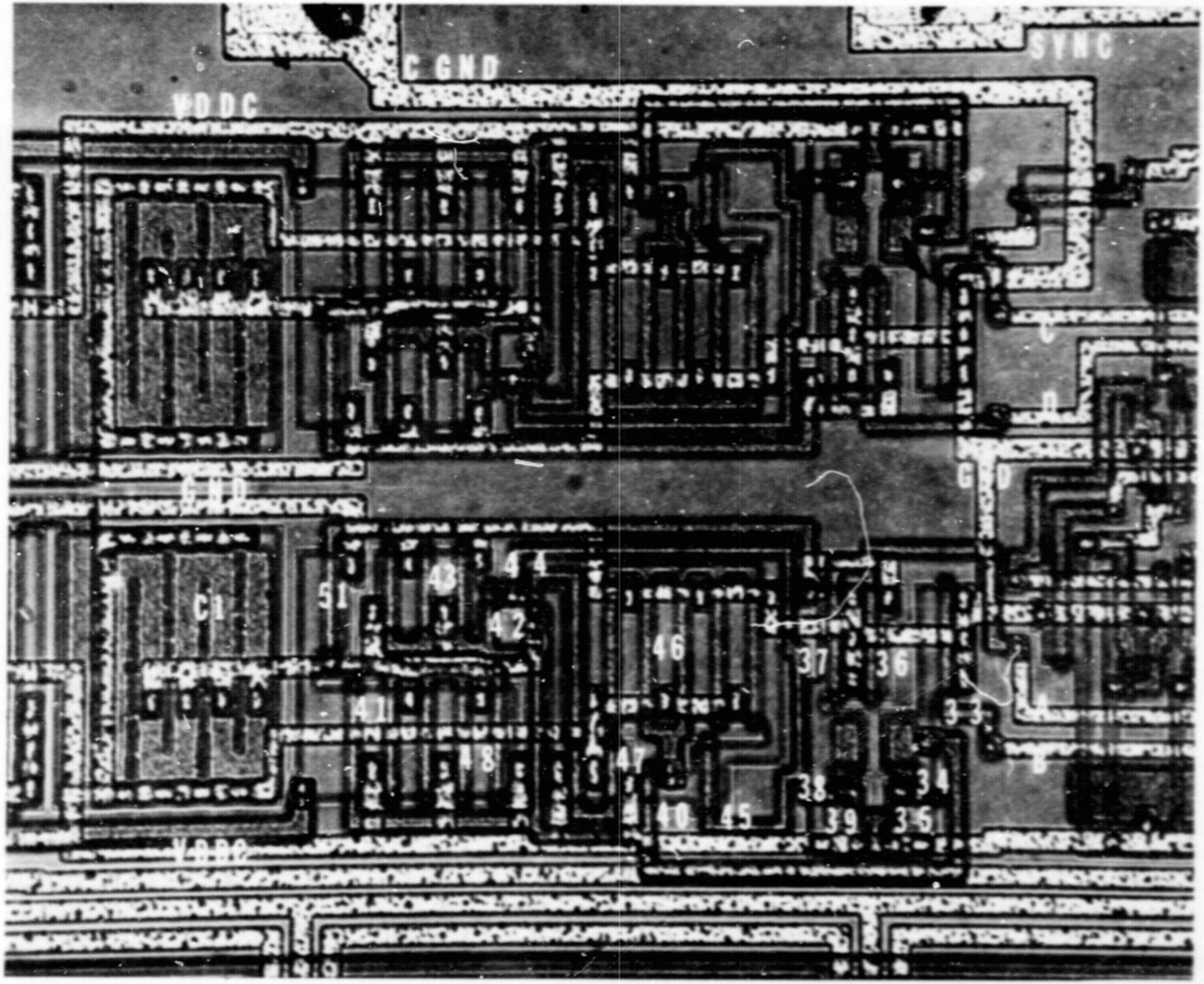


Figure IV-11 Clock Driver Circuit, R5101; X200

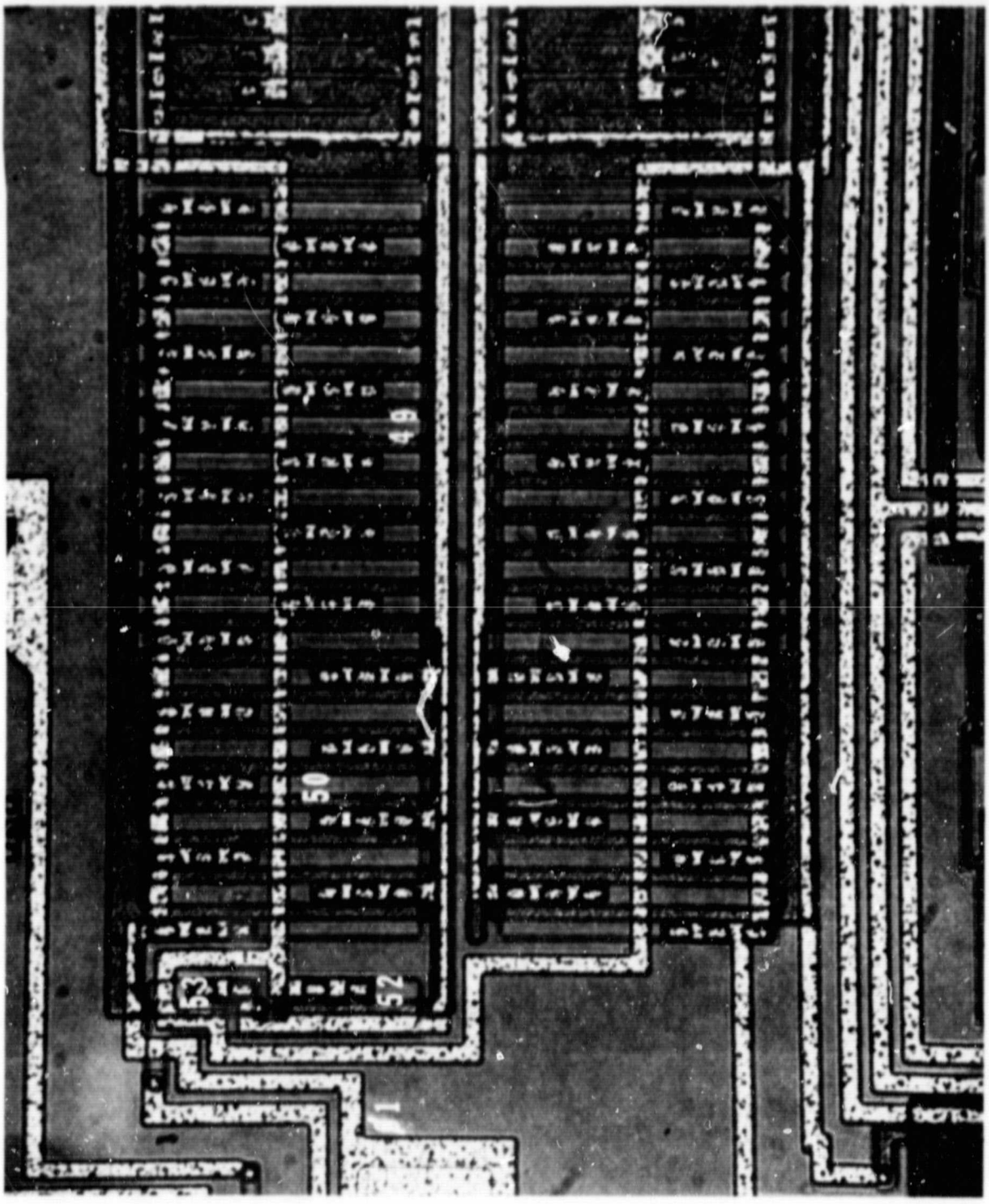


Figure IV-12 Clock Driver Output Circuit, R5101; X200

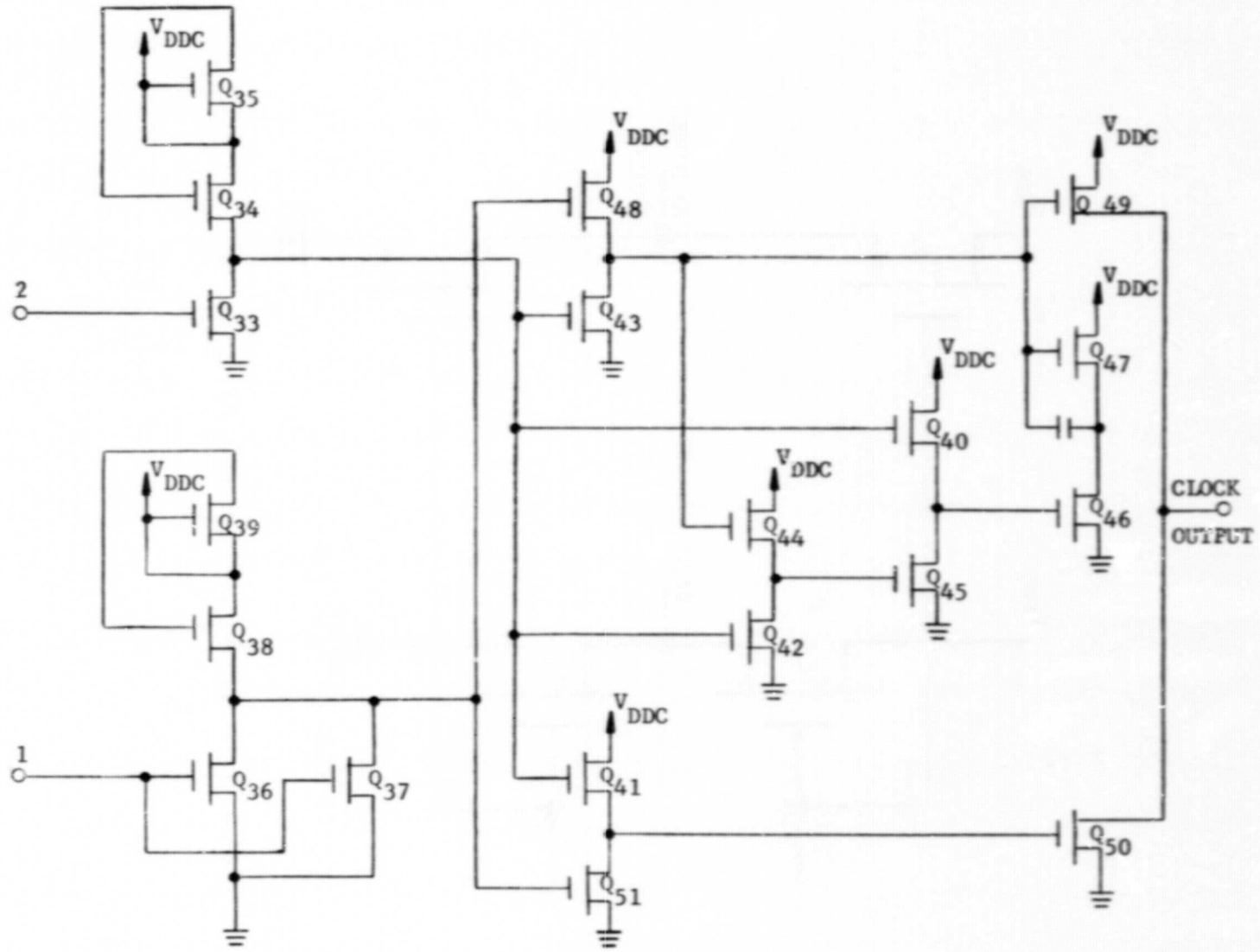


Figure IV-13 Schematic, Clock Driver, R5101

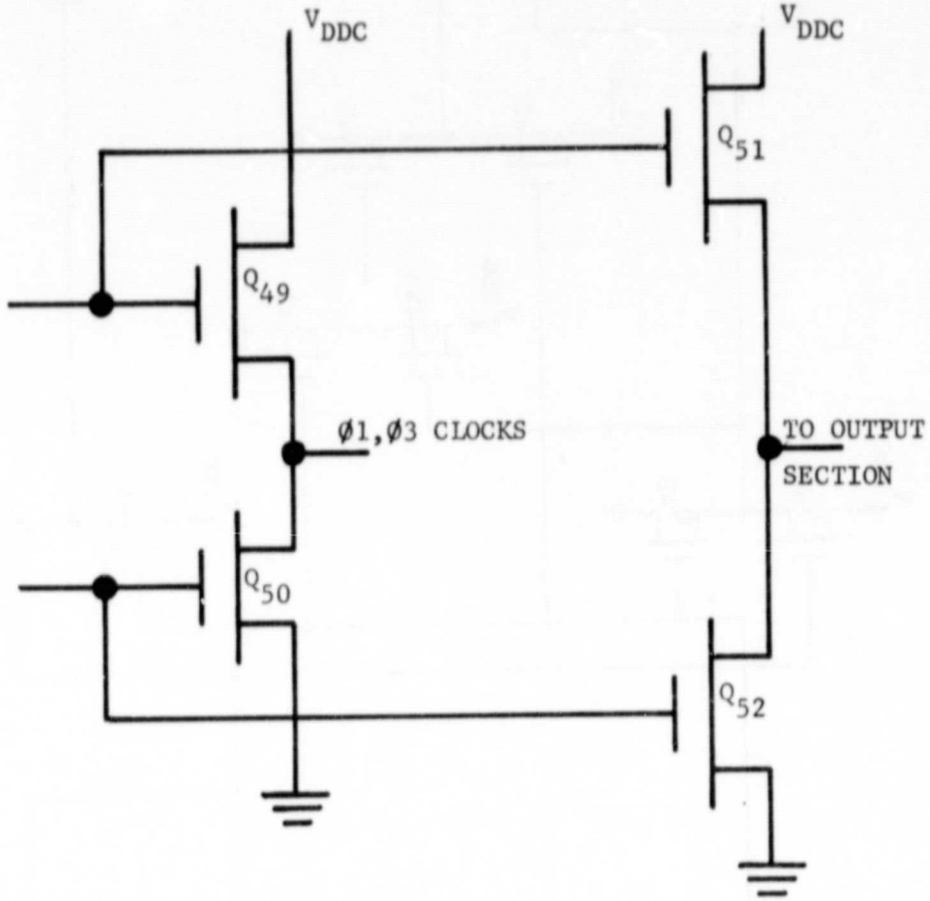


Figure IV-14 Clock Driver Output, R5101

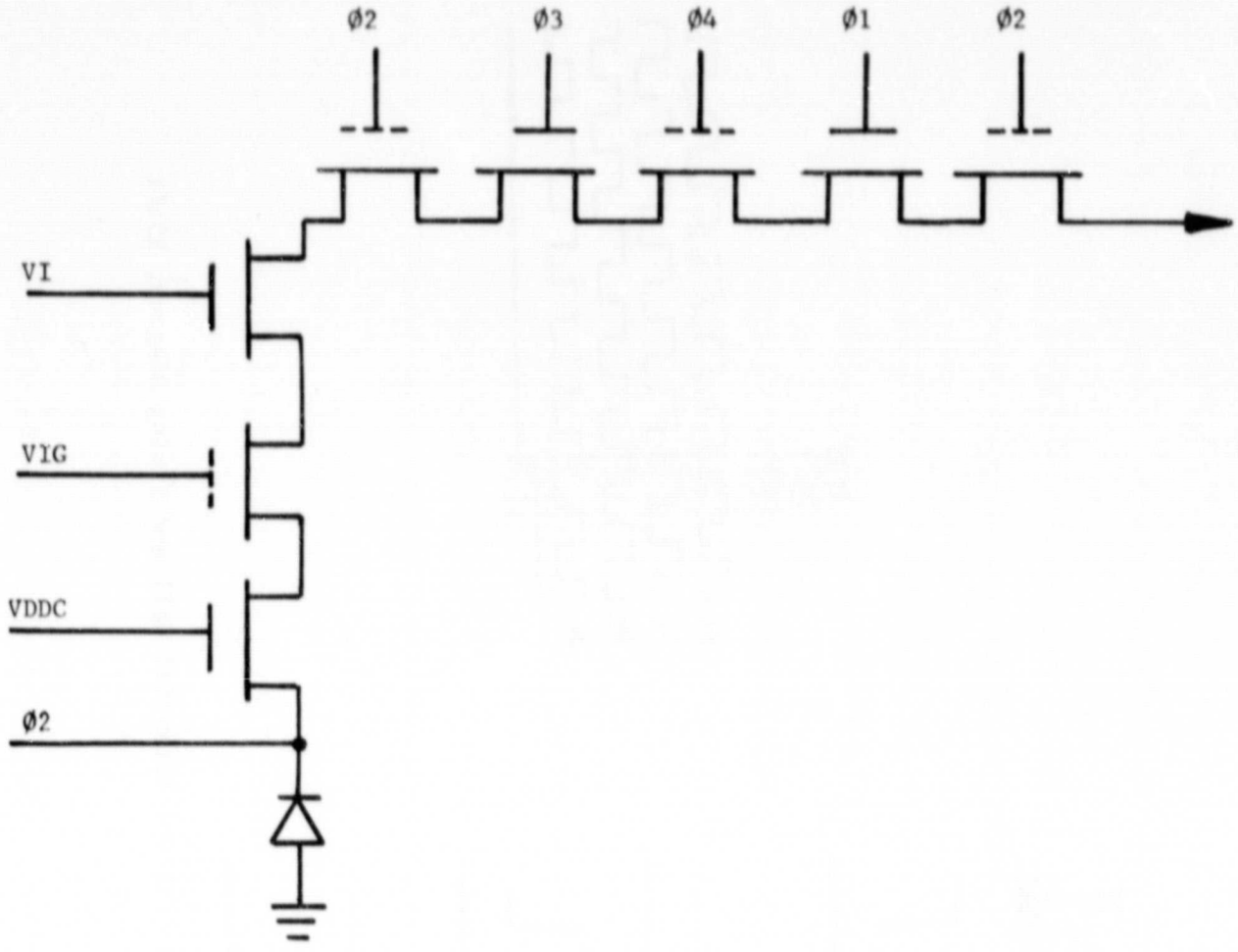


Figure IV-15 Schematic, Input Section, R5101

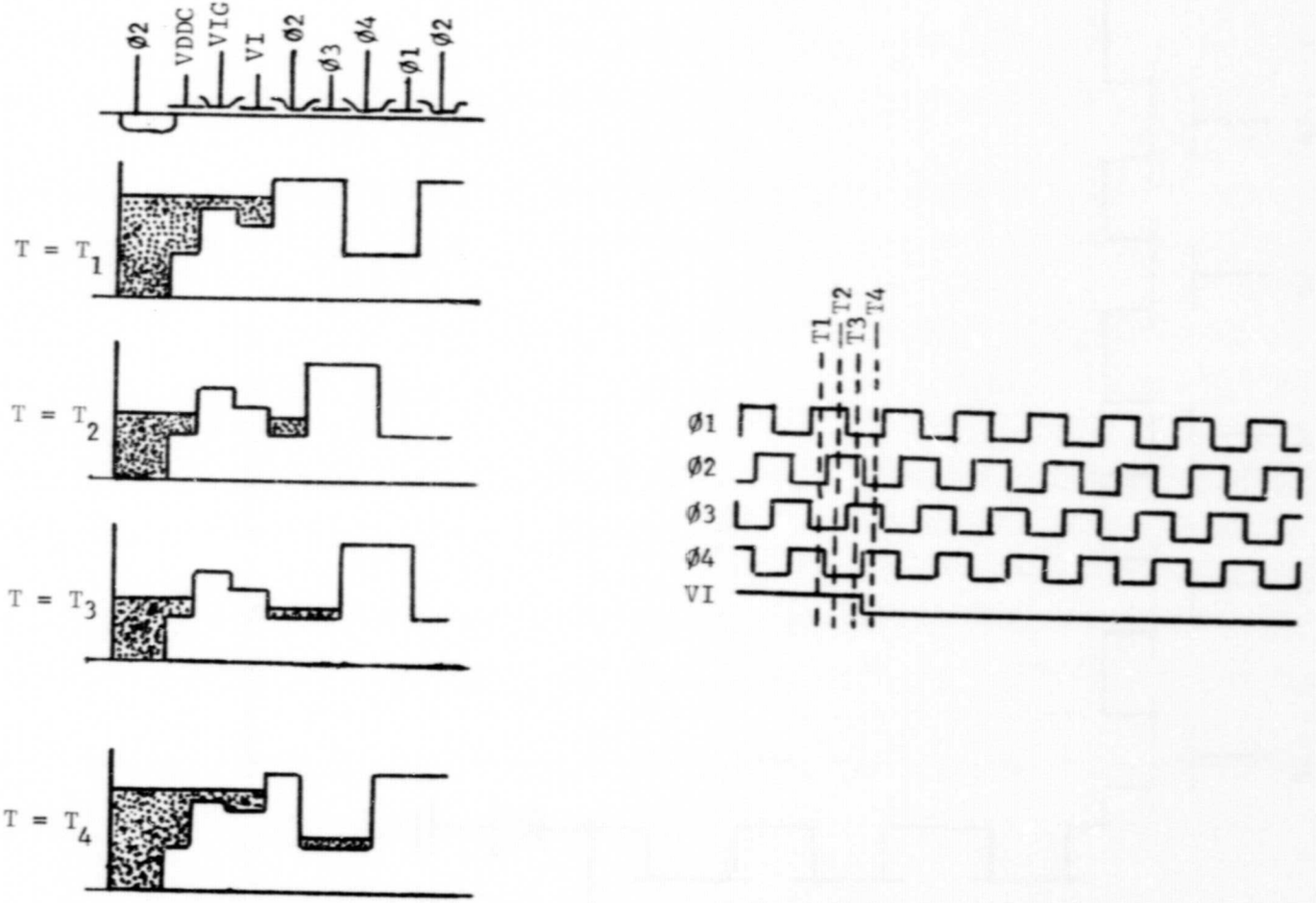


Figure IV-16 Input Cross Section, Potential Well and Timing Diagram, R5101

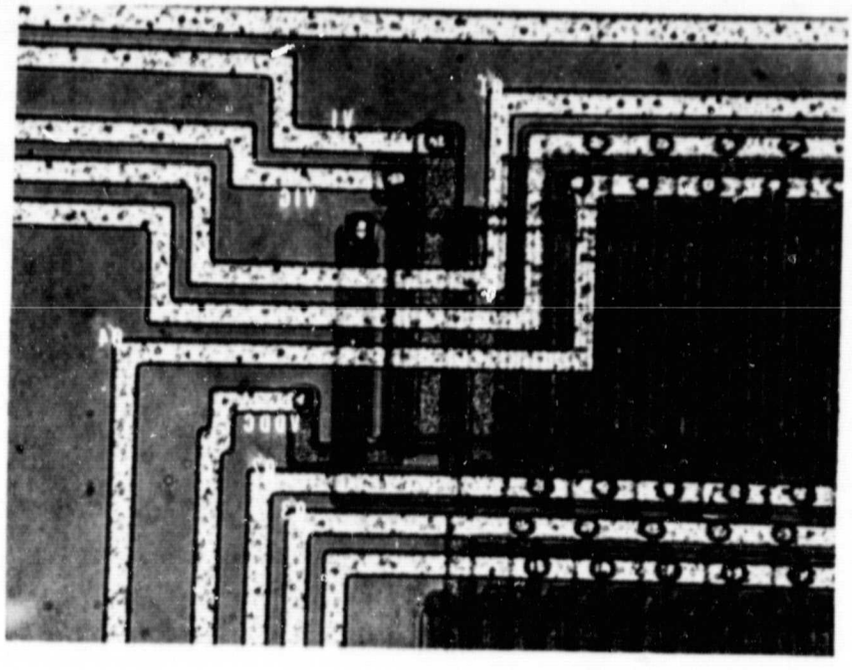


Figure IV-17 Input Circuit Photograph, R5101; X230

available to the CCD array. The data is therefore sampled on the $\phi 2$ rising edge. Since $\phi 2$ is now at a high potential a deeper well is formed under this electrode and the electrons which were under V_I will move to the area under $\phi 2$. At time T3, $\phi 3$ goes high and the charge spreads out under the $\phi 2$ and $\phi 3$ electrodes. At time T4, $\phi 4$ goes high and $\phi 2$ goes low. During this transition the charge is transferred from under the $\phi 2$ and $\phi 3$ electrodes to the area under the $\phi 3$ and $\phi 4$ electrodes. This process continues until the charge is completely transferred through the channel to the output section. Also occurring at time T4 is the sampling of another signal. The potential well under V_I is shallower in this case indicating a lower voltage on the gate.

c. Shift Register - The structure of the gates over the shift register was shown in the input circut section. The $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$ gates alternate the entire length of the channel with the exception of the corners. At each corner there is a floating n+ diffusion. At the input end of the diffusion is the $\phi 4$ electrode, and at the output end is a poly2 electrode (Figure IV-18). This poly2 gate is connected to a dc bias of 3 volts and is called V_{CB}, or corner bias. A charge packet will therefore reach the n+ diffusion when $\phi 4$ goes high. When $\phi 4$ goes low, this charge will flow through the n+ diffusion to the area beneath V_{CB} and the adjacent electrode $\phi 1$. The corner bias aids in the transfer efficiency at each corner. It is at a high enough potential to aid in the charge collection without retaining charge which should be transferred when $\phi 1$ goes high. The charge will then continue down the channel in the standard manner. A typical corner is shown in Figure IV-19. There are 17 separate columns to the channel with 16 corners. At the end of the channel two separate channels form and go to the output amplifier.

d. Output Amplifier - The output amplifier is shown schematically in Figure IV-20a and in the photograph in Figure IV-21. The timing diagram showing the relationship between the clocks and the output level is shown in Figure IV-20b. In the discussion of the input circuitry it was observed that the signal was sampled when $\phi 2$ was low and that the level was fixed at the time of the $\phi 2$ rising edge. This signal is then transferred through the channel to the output amplifier. When the channel splits half of the charge will go to each side at the time $\phi 1$ goes high. The charge is then transferred along these separate channels. At time T1 when $\phi 3$ goes high, an equal quantity of charge will more under the two gates labeled A and B. At this same time, with $\phi 3$ high, transistor Q4 will charge the gate capacitance of Q6. Since these are n-channel devices, the addition of the negative charge packet to the gate at time T2 will

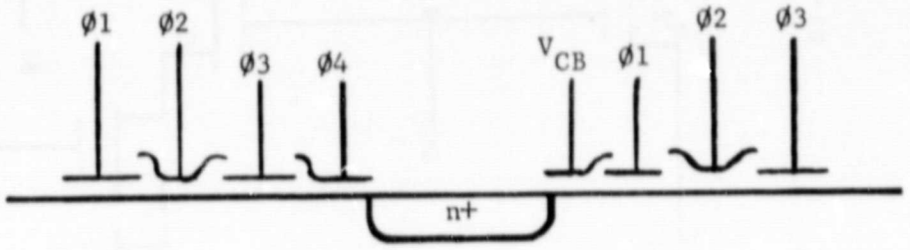


Figure IV-18 Corner Structure, R5101

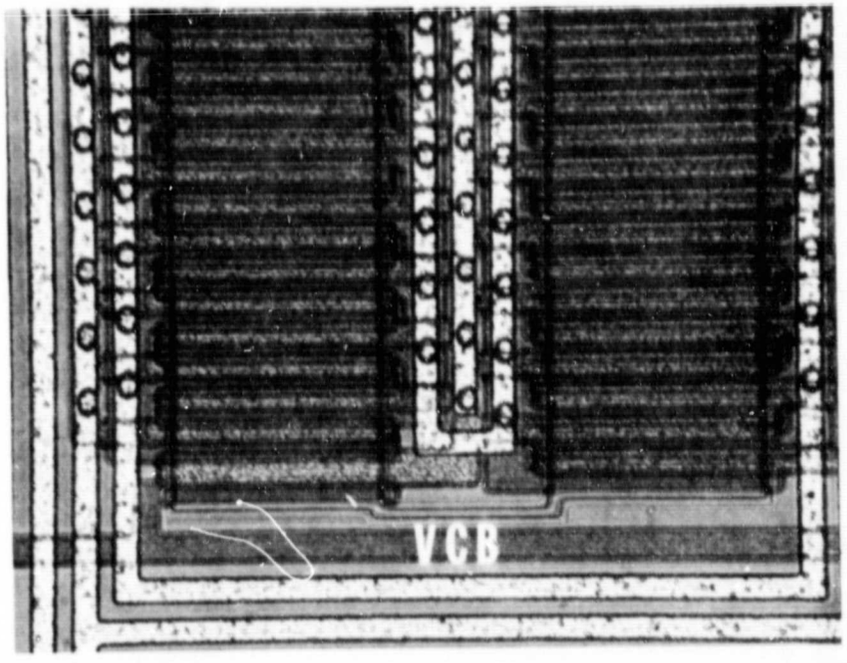


Figure IV-19 Corner Structure Photograph, R5101; X240

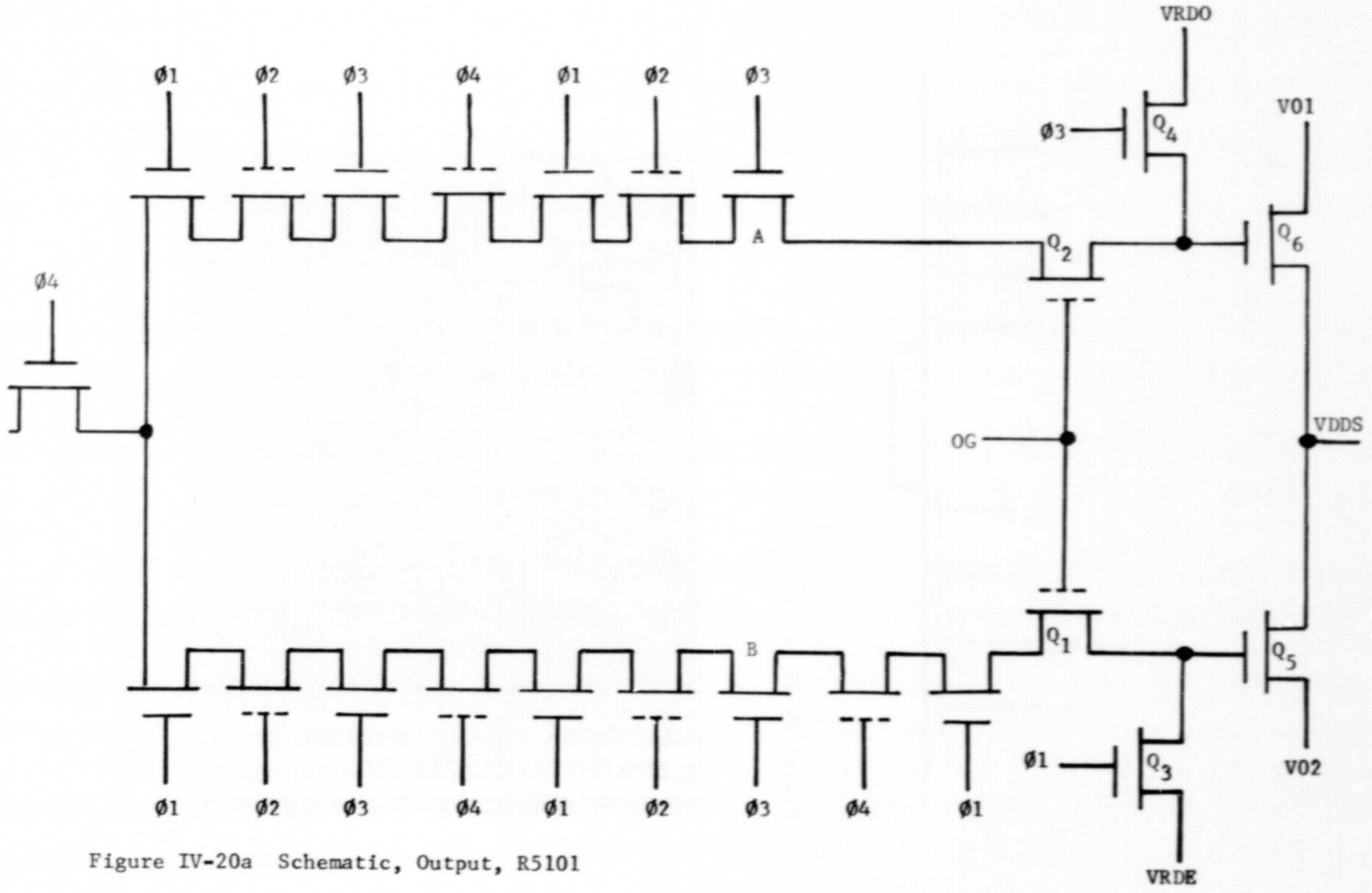


Figure IV-20a Schematic, Output, R5101

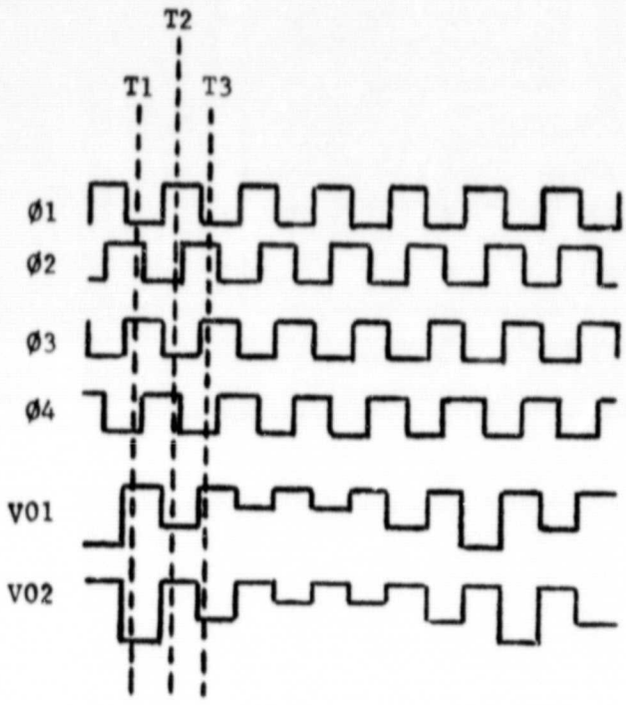


Figure IV-20b Output Timing, R5101

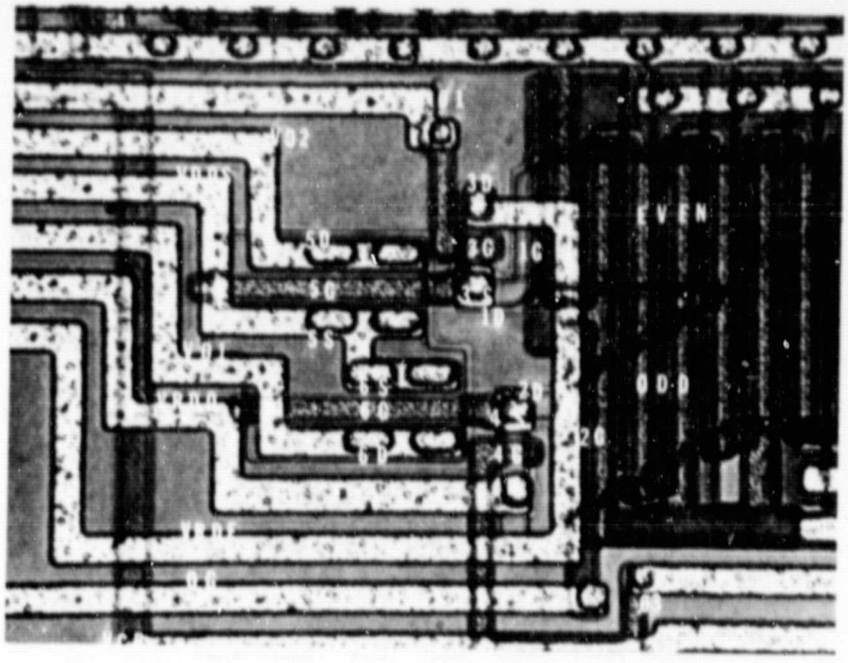


Figure IV-21 Output Circuit Photograph, R5101; X300

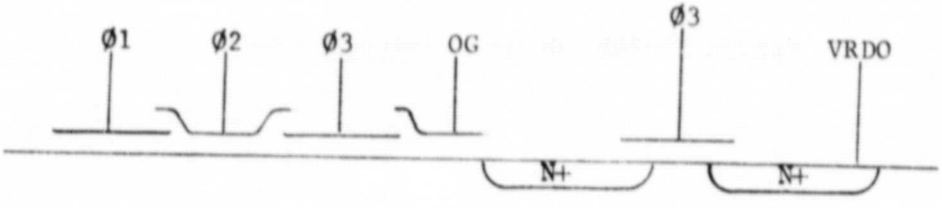


Figure IV-22 Output Cross Section, R5101

decrease the conduction of Q6. This results in the output voltage being lowered an amount proportional to the charge packet. The identical size charge packet which was at B at time T1 will be in the potential well under $\phi 4$ and $\phi 1$ at time T2. The even output, VO2, will be at its high reset value at this time. At time T3, VO2 will be at a level equal to that of VO1 at time T2. The shape of the output waveform is a sampled sinusoid in this Figure.

A cross-section of a portion of the odd output is shown in Figure IV-22. This shows the clock electrodes over the channel, followed by the OG electrode which transports the signal into the n+ diffusion. This diffusion is the common point between transistors Q2, Q4, and Q6 gate. The $\phi 3$ clock applies the V_{RDO} potential to this common diffusion. As can be seen from the cross-section and schematic, the transistors indicated in the channel and the OG transistor are only gate electrodes over a p-type material. The other four transistors in the output, Q3, Q4, Q5, and Q6 are standard silicon gate n-channel FET's.

e. Input Protect Circuit - Each of the inputs on this device which go to a gate has an input protect network. This is shown in the photograph in Figure IV-23 and schematically in Figure IV-24. The circuit consists of a diffused resistor which serves a combination of functions. It is an n-diffusion in a p substrate so it is a diode to ground, it is a resistive component to the signal that goes to the gates, and it is the drain diffusion for the FET shown. The FET has its source and gate tied together and these go to signal ground. A negative signal on the input would be connected to the substrate via the forward biased diode and also to signal ground when the FET conducts.

5. Scanning Electron Microscope Examination

A Cambridge S-180 SEM was used to examine the various layers on this device. The integrity of the metallization and the polysilicon layers were judged utilizing MIL-STD-883B Method 2018 as the criteria.

The passivation layer was examined and is shown in Figure IV-24. There was no evidence of cracking, peeling, or voiding which would degrade the effectiveness of this layer. A measurement of the passivation thickness was made at the edge of an opening for a contact window. This was found to be approximately 2 microns thick.

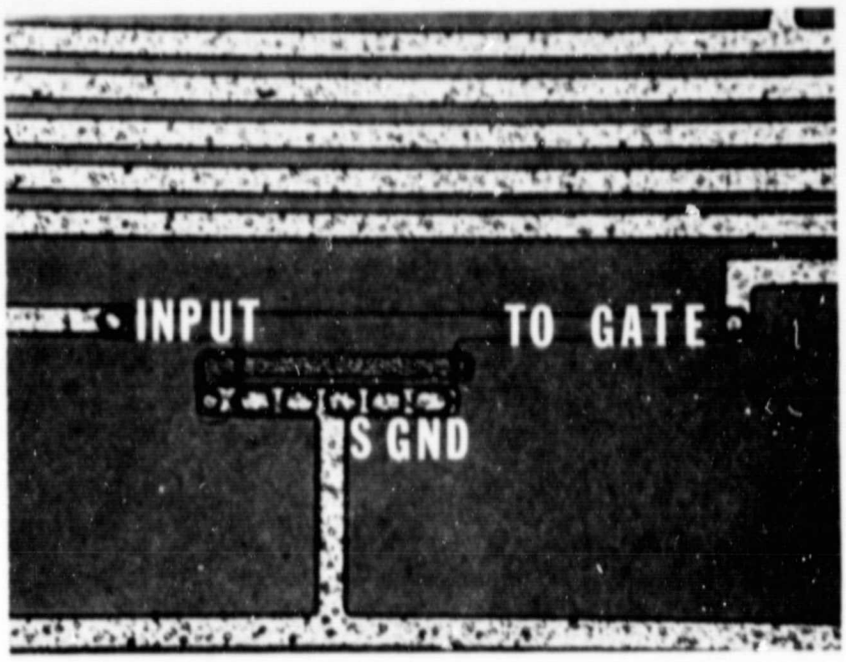


Figure IV-23a Input Protect Circuitry, R5101; X300

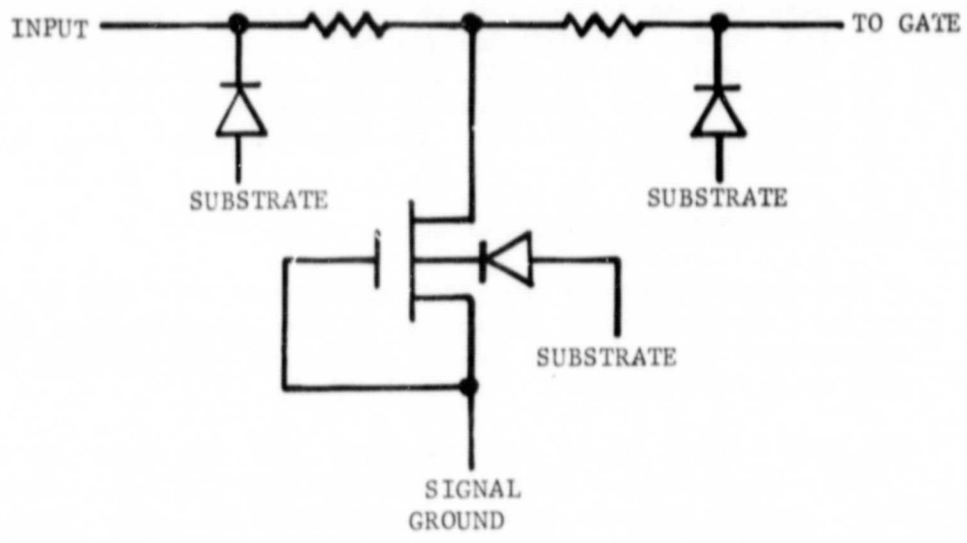


Figure IV-23b Schematic, Input Protect Circuit, R5101

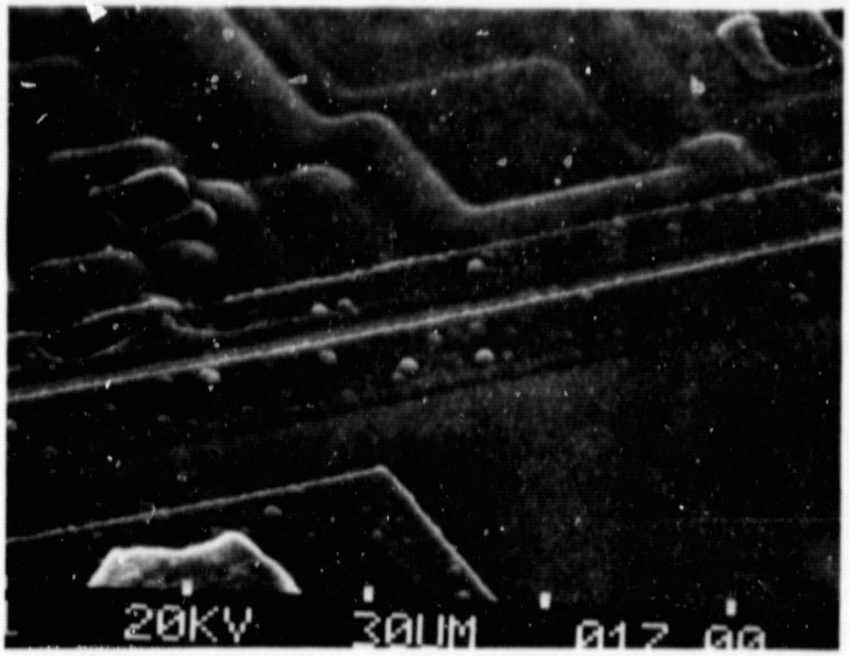


Figure IV-24 SEM Micrograph, Passivation, R5101; X830

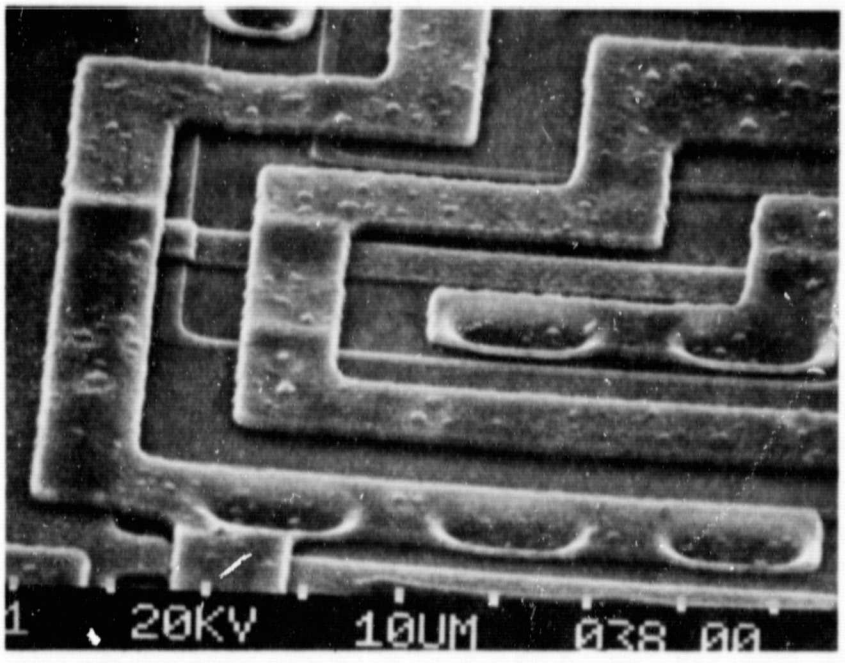


Figure IV-25 SEM Micrograph, General Metallization Coverage, X1300

Hydrofluoric acid fumes were used to remove the passivation to allow examination of the metallization and polysilicon layers. This etching process does not attack the metallization nor did it appear to attack the polysilicon. It did attack the oxide layer beneath the metallization and therefore gave it the appearance of being lifted or separated on the edge.

Examination of the metallization included the areas related to the clock circuitry, input circuitry, channel, output circuitry, and the input lines. All four directional edges were examined. An example of the general metallization appearance in the clock circuitry is shown in Figure IV-25. The metallization thickness was approximately 1 micron. This photo includes contact windows, step coverage over polysilicon, and step coverage over changes in the thermal oxide topography. There are no reliability problems evident in this SEM micrograph. Two more examples of the metallization coverage in the clock circuitry are shown in Figures IV-26 and IV-27. These are a combination of contact window and step coverage. There appears to be a relationship between the direction of the step and the step coverage. Figure IV-26 has very good coverage and Figure IV-27 has a small crack or etch appearance along the edge of the bottom step. The coverage on both is acceptable. The directional effect showed up again in the channel metallization. Figure IV-28 is the general metallization appearance and Figure IV-29 is the worst case contact window seen. The metallization step over the polysilicon in this direction was found to have a more noticable crack along the edge. Referring to Figure IV-28 there are three metallization stripes which contact polysilicon. The center stripe contacts the lower level polysilicon (poly1) and the two outside stripes contact poly2. If the contact windows on the poly2 had been shifted slightly the contacts could have been made in an area without a step. This would have alleviated the condition seen in Figure IV-29. There were no step coverage problems seen which could be considered rejectable. The aluminum metallization was then removed with commercially available Transene Aluminum Etchant. The polysilicon layers on all areas of the chip were then examined and documented.

Figure IV-30 shows the appearance of the general polysilicon coverage. The large polysilicon stripe with the contact windows on the left hand side of the picture is a poly2 layer. This is the layer which is connected to the Ø2 clock. The step which occurs in approximately the center of the photograph going from the top to the bottom is the edge of the channel, with the channel being on the right. Starting at the contact window on the polysilicon in the middle of the picture the Ø2 clock can be followed over to the channel region. Proceeding downward the next clock is the Ø3 clock (poly1). This comes from the left hand side of the picture and

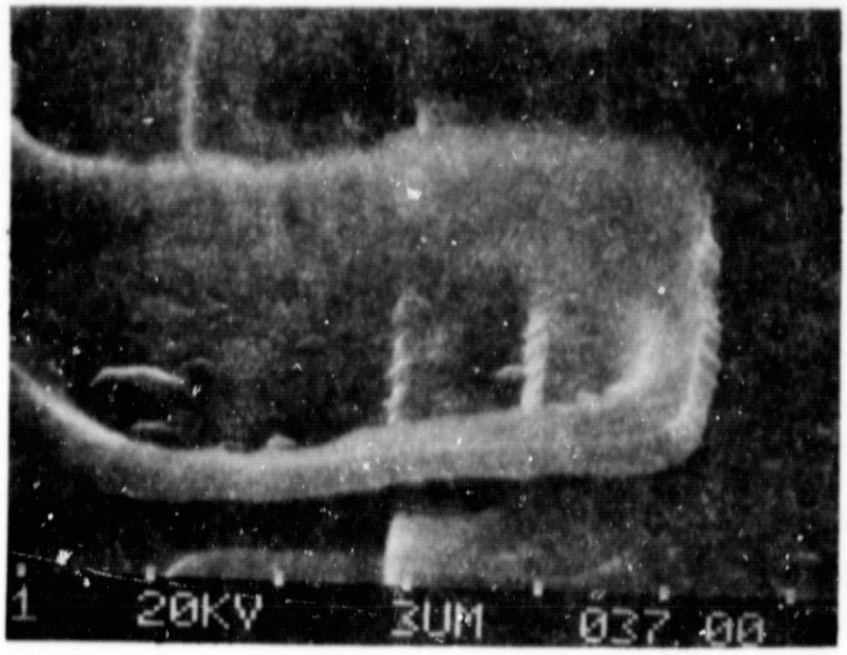


Figure IV-26 SEM Micrograph, Metallization Step Coverage, R5101; X6000

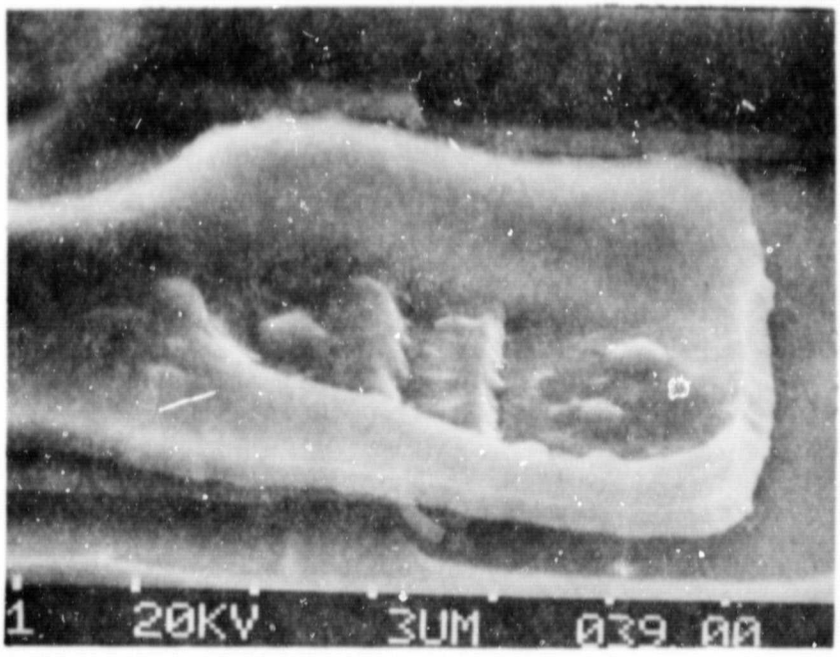


Figure IV-27 SEM Micrograph, Metallization Step Coverage, R5101; X5500

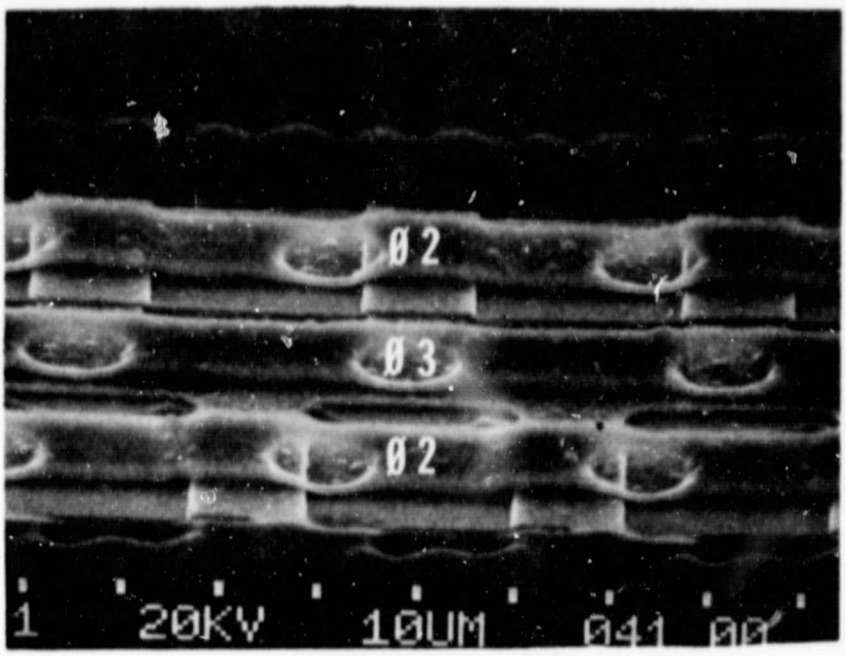


Figure IV -28 SEM Micrograph, General Metallization Coverage; X1400

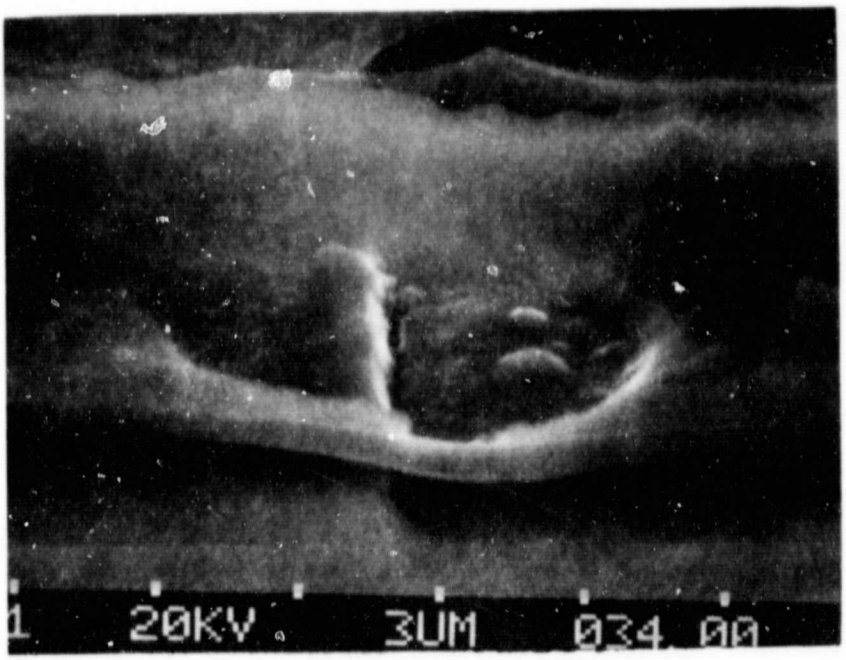


Figure IV-29 SEM Micrograph, Contact Window Metallization Coverage; R5101; X6600

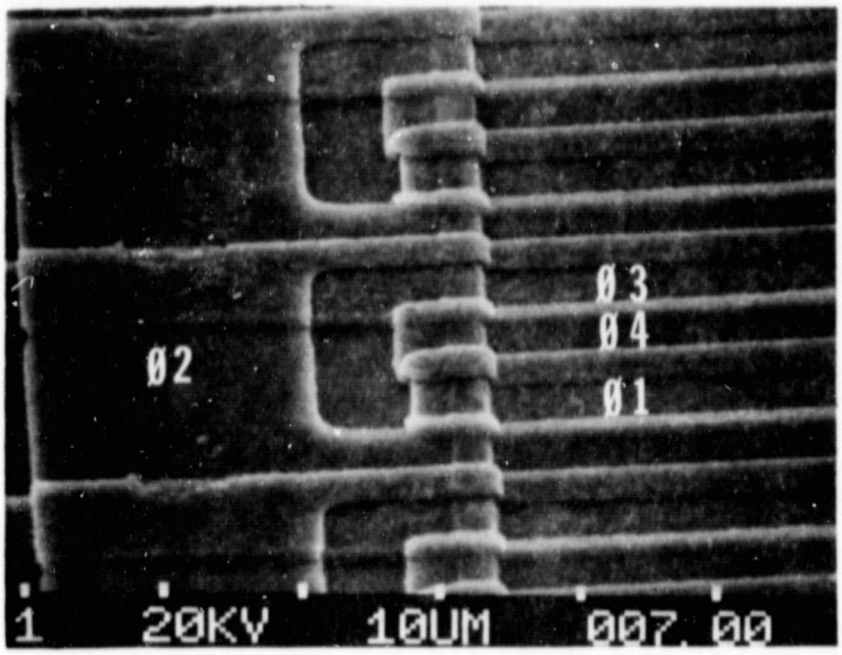


Figure IV-30 SEM Micrograph, General Polysilicon Coverage, R5101; X2000

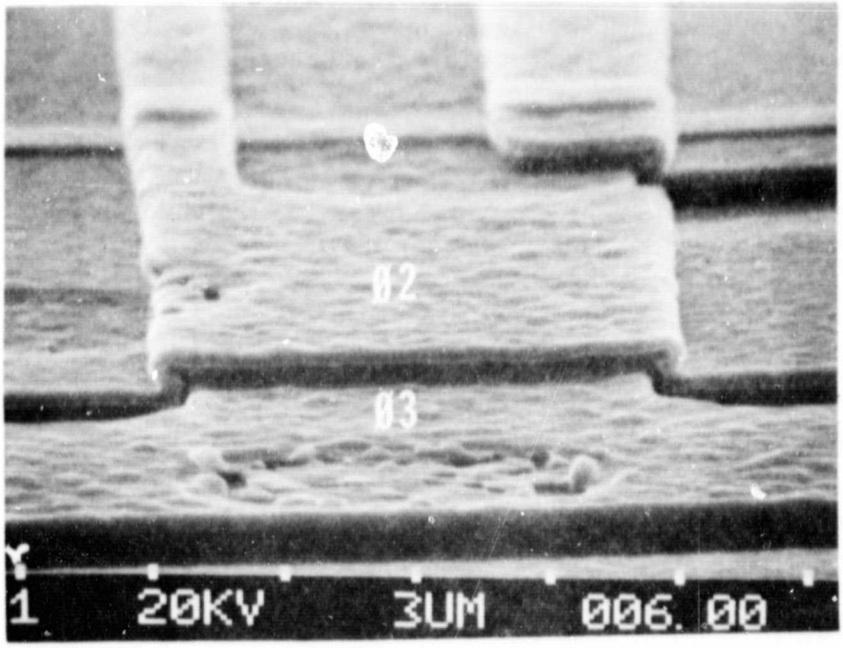


Figure IV-31 SEM Micrograph, Polysilicon Step Coverage, R5101; X6000

corresponds to the center metallization stripe seen in Figure IV-28. The next polysilicon layer comes from the right hand side of the photograph and is the ϕ4 clock (poly2). The last one in the series before they repeat is the ϕ1 clock (poly1).

Higher magnification documentation of the polysilicon layers shown in the SEM micrographs in Figures IV-31 thru IV-34. Figure IV-31 is a photograph taken at 90 to Figure IV-30 with an increased tilt angle. At the bottom of the picture is the ϕ3 clock line which is then traversed by the ϕ2 clock line and the ϕ4 clock line is in the upper right hand corner. Note the extremely good step coverage of the ϕ2 line over the ϕ3 line. Figure IV-32 is of the ϕ4 clock line at the edge of the channel. This is a poly2 layer and it shows very good step coverage over both the thermal oxide step and the poly1 layer. Figure IV-33 shows several polysilicon steps as well as the thicknesses of the layers involved. The top layer of polysilicon (poly2) is approximately 0.4 microns thick. This is separated from the bottom polysilicon layer by approximately 0.5 microns of dielectric. The poly1 layer is approximately the same thickness as the poly2 layer. Again note the extremely good step coverage and uniform film thickness of the poly2 layer. Figure IV-34 is an example of a poly1 layer in the clock circuitry where a contact to the aluminum metallization had been made. Note the uniformity of the film thickness over the thermal oxide step.

During the SEM examination of the conducting layers on this device there were no layers seen which were unacceptable.

6. Diffusions and Polysilicon Conductors

This section will discuss the diffusions used on this chip and will show these diffusions and the polysilicon conductors in cross-section.

There are five areas on the chip that are produced by an n+ diffusion. These are the clock circuitry, the input diode, the corner diffusion, the output amplifier, and the input protect circuit. The top view of these areas with all of the conductor layers chemically removed and the diffusion stained is shown in Figures IV-35 thru IV-39. Figure IV-35 shows a portion of the output on the clock circuitry. These are alternating source and drain diffusions for the clock driver transistors. Figure IV-36 shows the input diode. This diode is connected to ϕ2 and provides the source of charge for the channel. Figure IV-37 shows the corner diffusion. This will transport the charge from one column to the next. Figure IV-38 shows the output amplifier diffusions. These are identical for the two separate channels. Figure IV-39 shows an input protect circuit. The contact windows on either end of the long diffusion are the input and output for the protect resistor. The smaller diffusion with the 5 contact windows goes to ground.

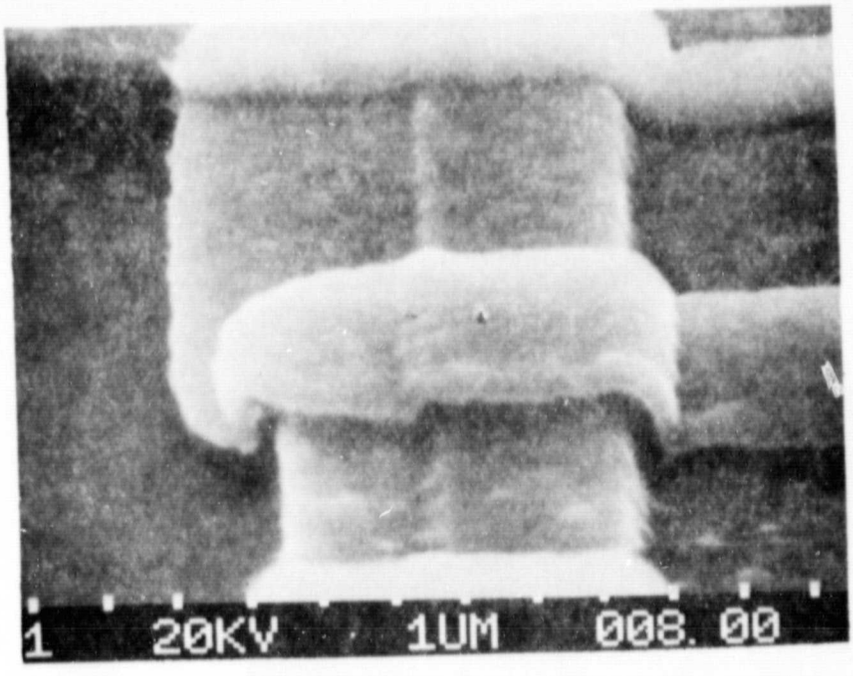


Figure IV-32 SEM Micrograph, Polysilicon Step Coverage, R5101; X10,000

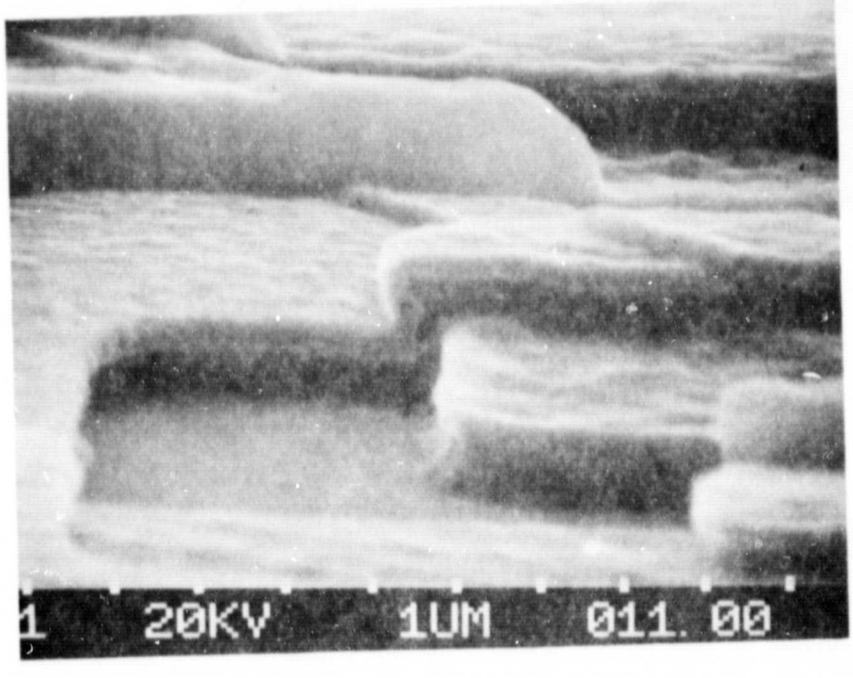


Figure IV-33 SEM Micrograph, Polysilicon Step Coverage, R5101; X12,000

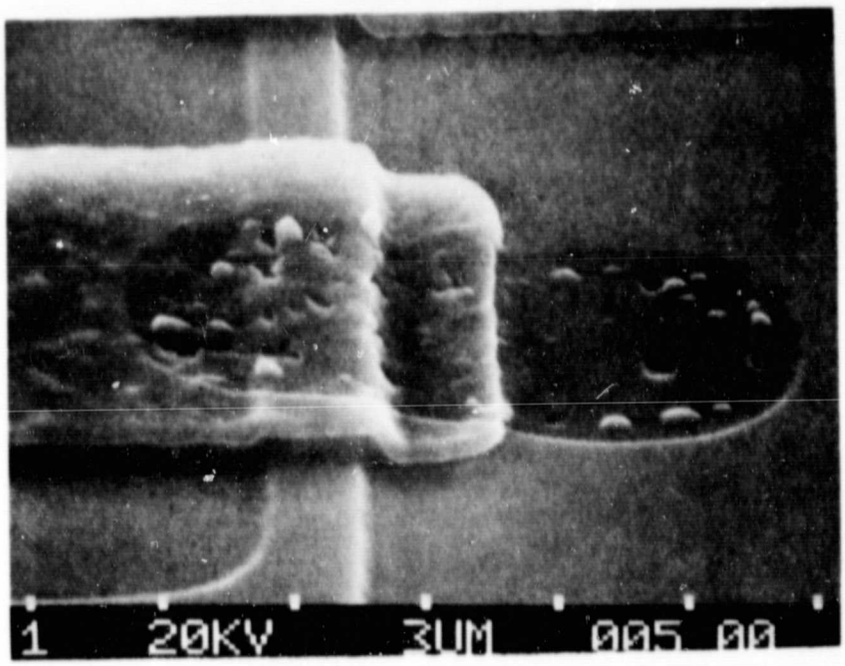


Figure IV-34 SEM Micrograph, Polysilicon Step Coverage, R5101; X6000

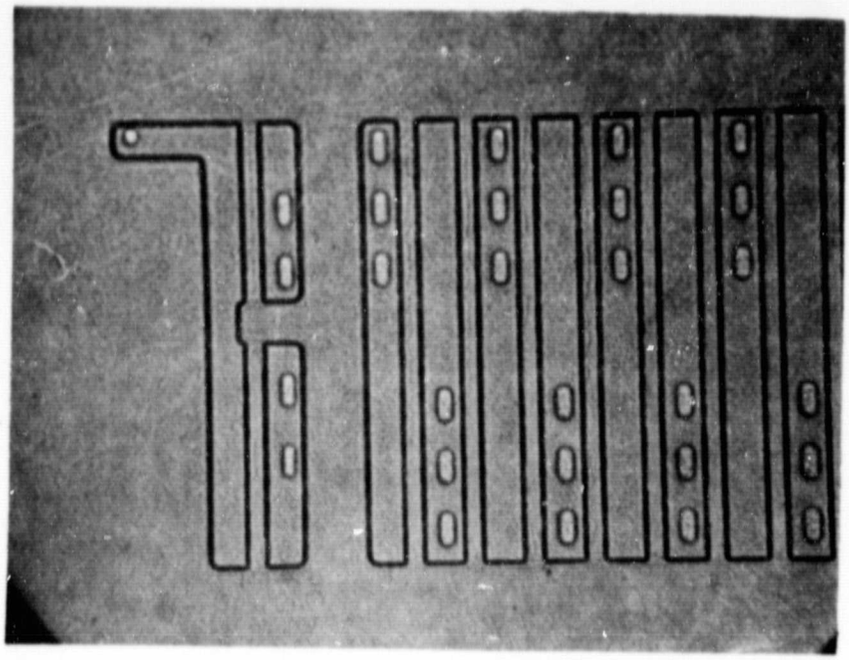


Figure IV-35 Clock Circuitry Diffusions, R5101

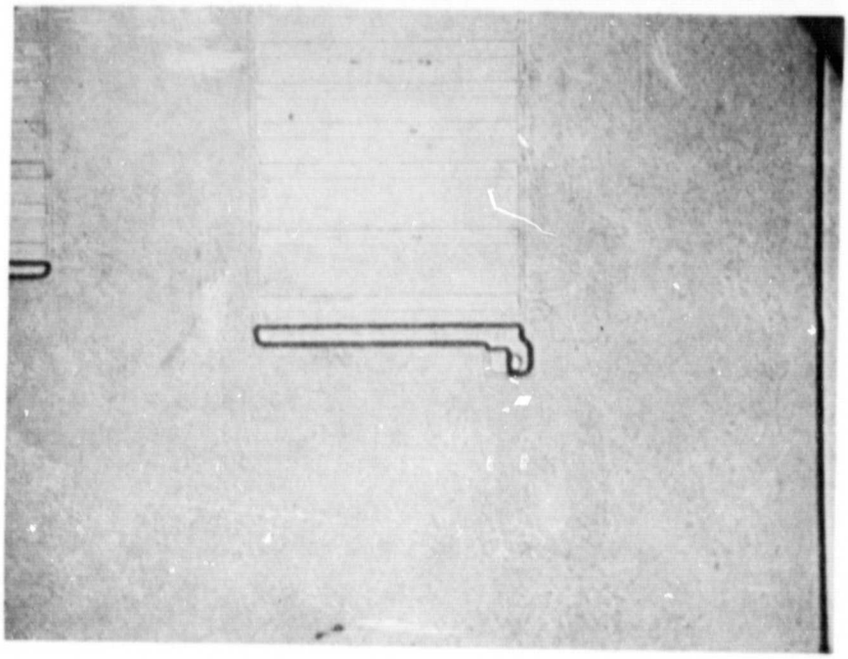


Figure IV-36 Input Diode Diffusions, R5101

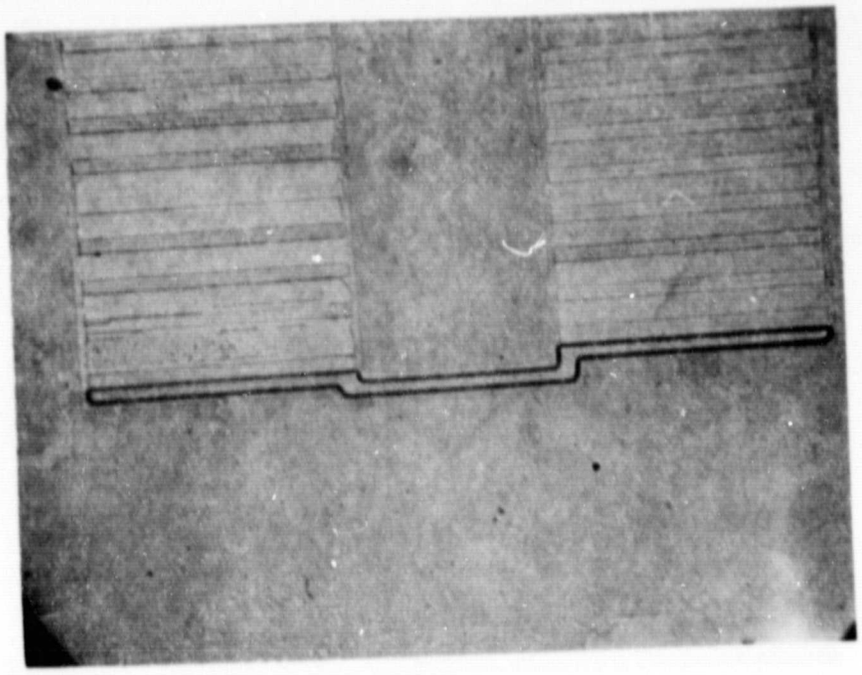


Figure IV-37 Corner Diffusion, R5101

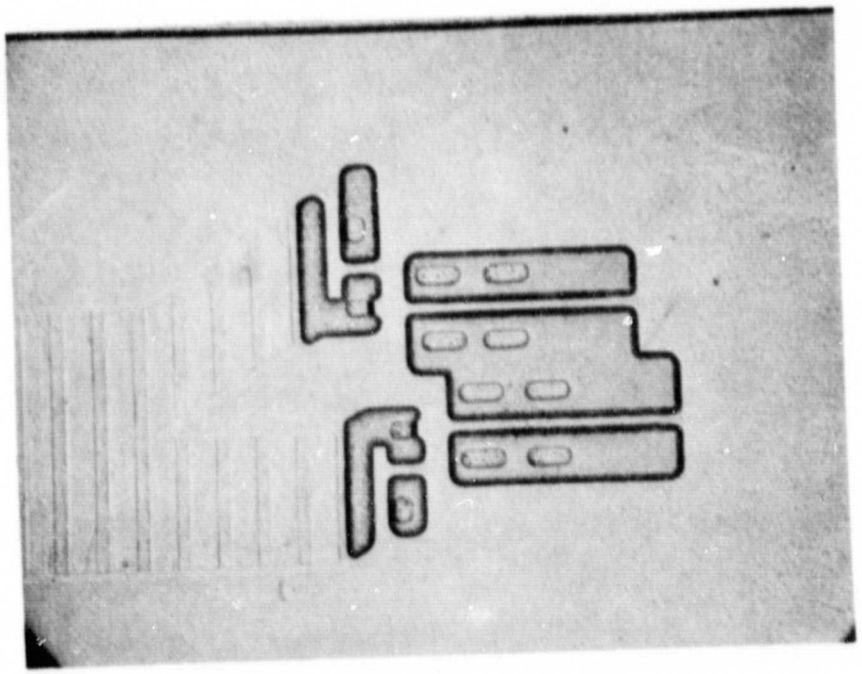


Figure IV-38 Output Diffusions, R5101

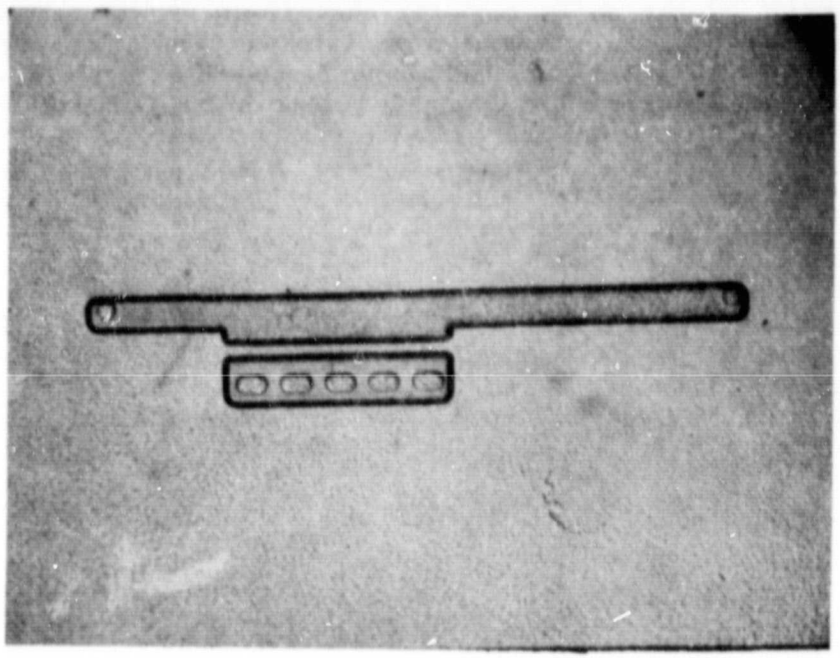


Figure IV-39 Input Protect Diffusions, R5101

The n+ diffusion is shown in cross-section in the photographs in Figures IV-40 thru IV-42. Figures IV-40 and IV-41 are on the same die and are areas of the clock circuitry. Figure IV-40 shows three diffused areas with polysilicon gates and one metallization contact point. The diffusions are approximately 5 microns thick. Figure IV-41 shows another section in the clock circuitry. The two polysilicon conductors on the right are transistor gates and the two polysilicon conductors on the left are separated by additional thermal oxide from the silicon and are not used as transistor gates at this point. Figure IV-42 is on a different die than Figures IV-40 and IV-41. This shows a diffusion on a corner. This has a different appearance due to a difference in the angle of the microsection and the length of the etch. Lateral confinement of the shift register channel is provided by a p+ diffusion. This could not be identified in the cross-section analysis, however, the Reticon personnel supplied the following information. The active areas are surrounded by a p+ diffusion with a surface concentration of about $3 \times 10^{16}/cm^3$. This is approximately 3 microns wide and 1 micron deep. The p substrate is approximately $2 \times 10^{15}/cm^3$.

Figure IV-43 shows the overlapping structure of the polysilicon in the channel region. This section is taken almost parallel to the channel region. The right hand side of the photograph where the polysilicon is close to the silicon is the shift register channel. The left hand side is between channels.

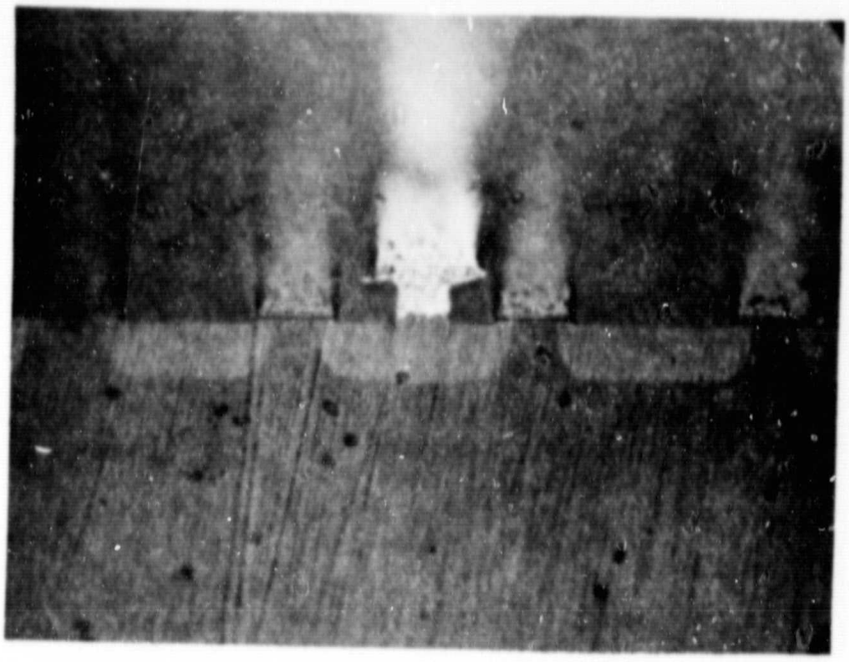


Figure IV-40 Diffusion Cross Section, R5101; X1200

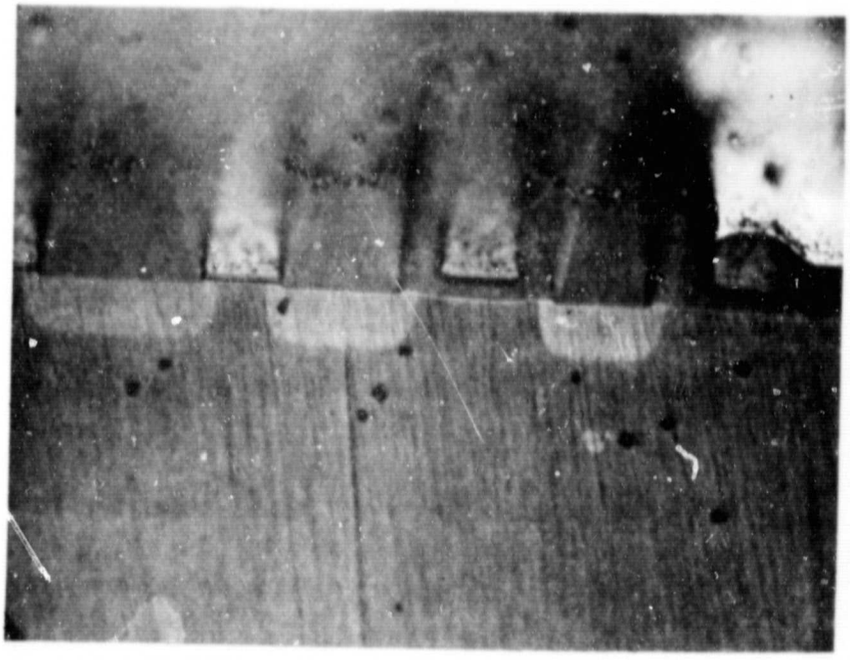


Figure IV-41 Diffusion Cross Section, R5101; X1200

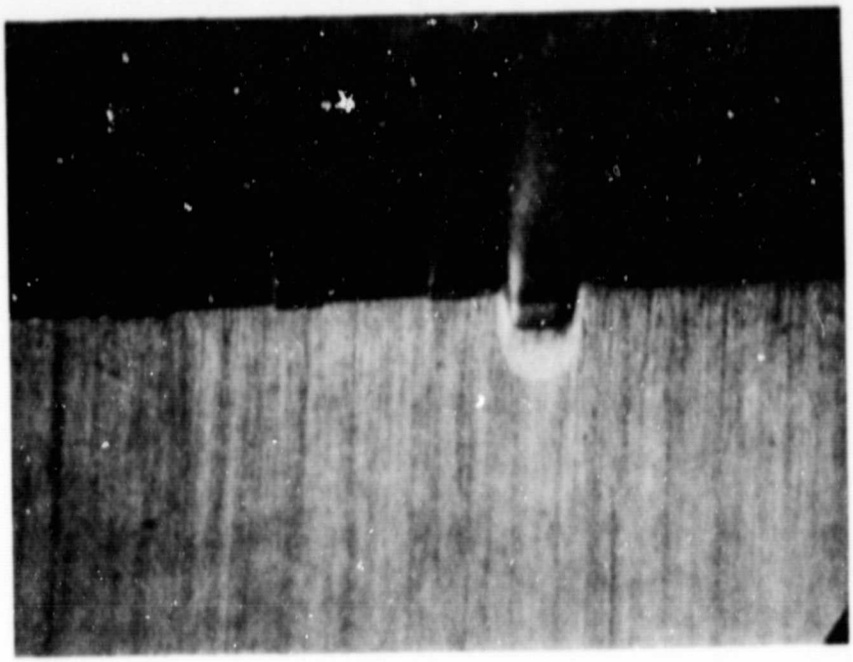


Figure IV-42 Diffusion Cross Section, R5101; X1000

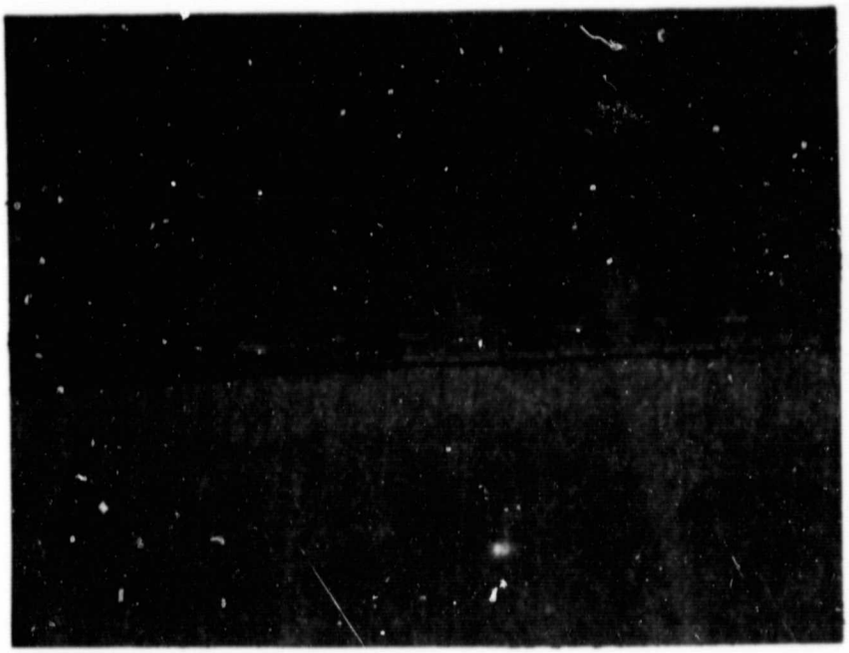


Figure IV-43 Polysilicon Structure, R5101; X1000

B. Electrical Characterization - General

The manufacturer's data sheet is included in the appendix. The Reticon R5101 devices were obtained directly from the Reticon Corporation in Sunnyvale, California. The first order of parts arrived in non-hermetic epoxy packages. These were returned to Reticon and were replaced with ceramic dual-in-line packages.

1. Operating Parameters

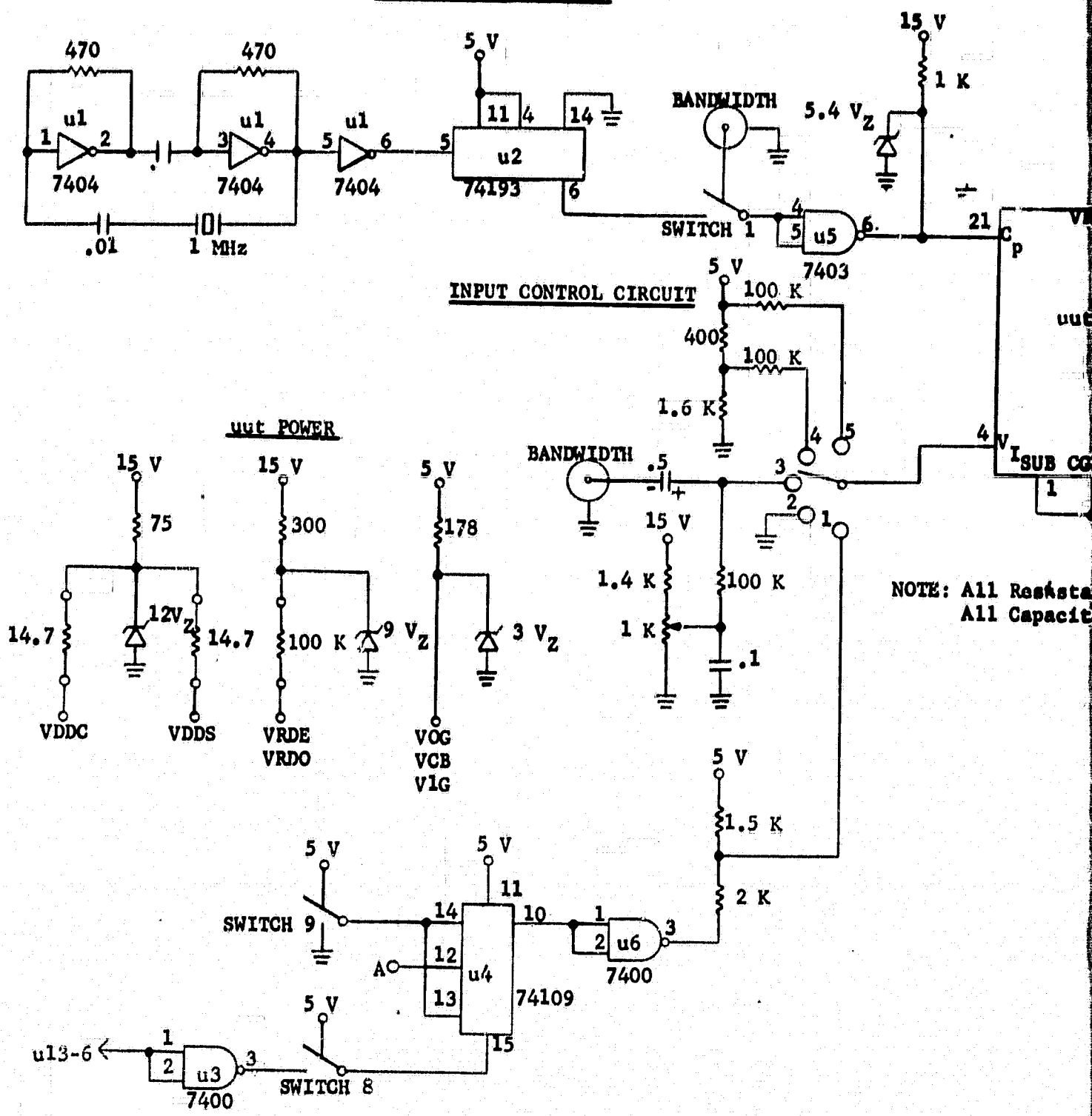
Upon receipt the R5101 circuits were electrically characterized to determine their operating range. They were operated in the test tool shown in Figure IV-44. This tool was designed specifically to operate the R5101 and perform the electrical tests to be described in this section. The voltages and signals required to operate this circuit are shown in Figure IV-44 and in the table from the data sheet, Table IV-2.

In Table IV-2 the first function is the clock voltage. This clock voltage is a square wave in Figure IV-44 with an amplitude of 5.4 volts and a frequency of 125 KHz. This voltage level is non-critical and can range from 5 volts up to V_{DD}. This clock controls the operating frequency of the device. It is used to drive the four-phase clock and driver section on the chip. The relationship of the timing on Cp and the internal clocks was shown in Figure IV-9. The delay time between the edge of the Cp input and the corresponding rise or fall of the clock signal is specified in the data sheet as typically 100 nanoseconds.

The sync pulse voltage is the next function in Table IV-2. In the test tool the sync input, pin 22 in connected to ground. This input allows several R5101 circuits to be operated with the same relative timing between phase clocks. The timing associated with the sync input is shown in Figure IV-9. There should be a minimum of 100 nanoseconds between the time $\phi 3$ goes high and the time the sync input goes high. For electrical test of a single circuit the sync input should be checked for input leakage but for the remainder of the tests it should be connected to ground.

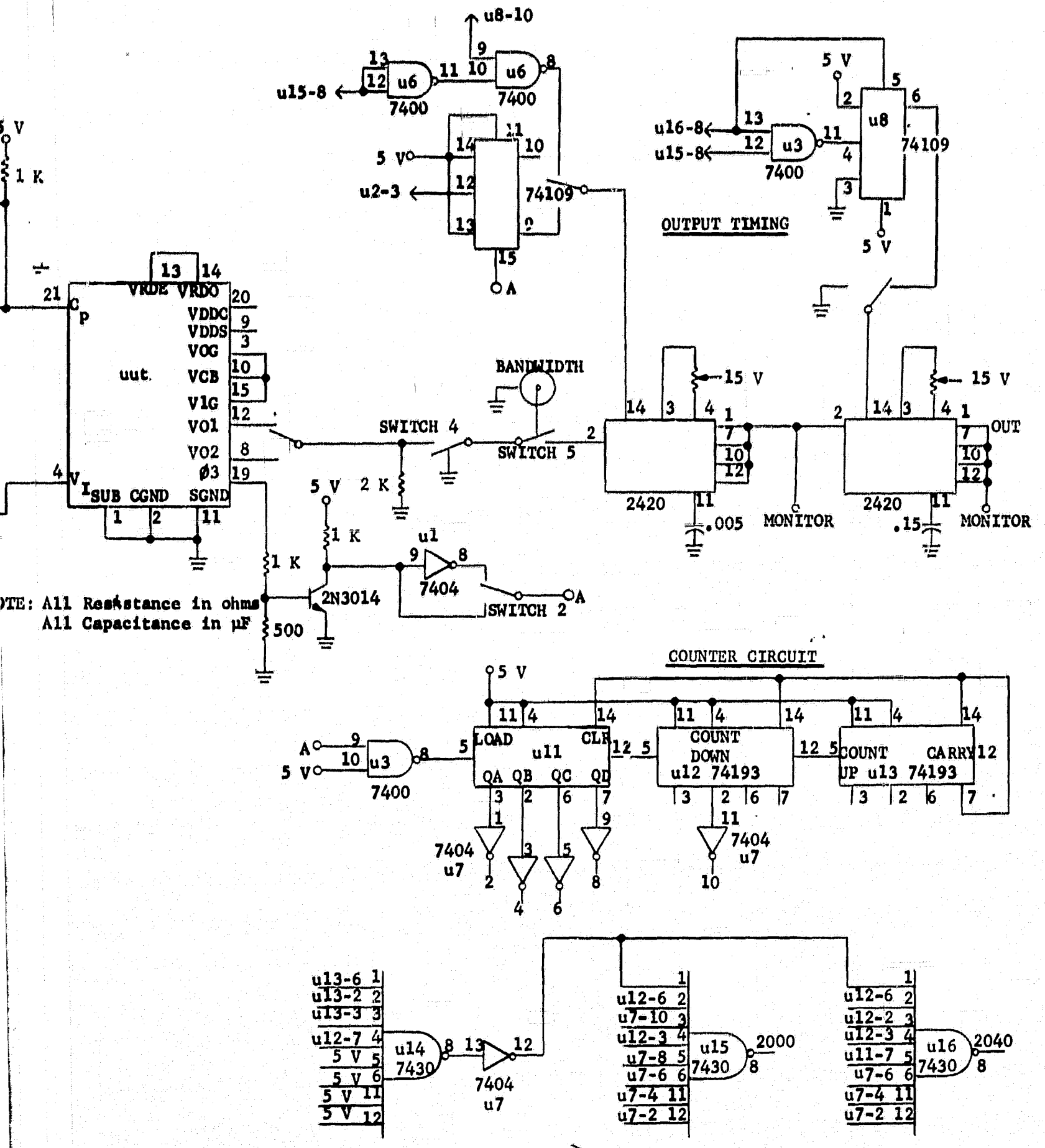
The output bias, pin 15, is set at 3 volts in the test tool. The bias is the gate voltage on the FET that transfers the charge from the shift register to the output amplifier.

The corner bias, pin 10, is also set at 3 volts in the test tool. This bias is connected to an electrode on each corner of the shift register and allows charge to be transferred from one row of the register to the next.



FOLDOUT FRAME

PRECEDING PAGE BLANK NOT FILMED



FOLDOUT FRAME

Figure IV-44 Schematic, Test Tool, R5101

TABLE IV-2 OPERATING SPECIFICATION, R5101

FUNCTION	SYMBOL	PARAMETER			UNITS
		MIN.	TYPICAL	MAX.	
Clock Voltage	V_{CP}	5		VDD	Volts Peak
Sync Pulse Voltage	V_{SYN}	5	10	VDD	Volts Peak
Output Bias	V_{OG}	1	3	4	Volts dc
Corner Bias	V_{CB}	1	3	4	Volts dc
Input Isolation Bias	V_{IG}		3		Volts dc
Analog Input Bias	V_I	3		6	Volts dc*
Signal V_{DD} Voltage	V_{DDS}		12	15	Volts dc
Driver V_{DD} Voltage	V_{DDD}		12	15	Volts dc
Signal V_{DD} Current	I_{DDS}		8		ma
Driver V_{DD}Current	I_{DDO}		8		ma
Reset Drain Voltage Odd	V_{RDO}		9		Volts dc
Reset Drain Voltage Even	V_{RDE}		9		Volts dc
Reset Drain Current Odd	I_{RDO}		70		μamp
Reset Drain Current Even	I_{RDE}		70		μamp
Clock output	$\emptyset_3$				see text,
Signal Outputs	V_{01} and V_{02}				

The input isolation bias, pin 3, is the third lead connected to 3 volts on the test tool. This bias produces a potential well of the correct depth to isolate the charge source on the input from the analog signal potential well. This is discussed in detail in the construction analysis section.

The analog input bias is applied to pin 4 on the R5101 and is the device input signal. On the test tool this can be switched to 5 different positions. The purpose of each position will be discussed in the appropriate electrical measurement section. For initial characterization of the devices position 3 was used and a D.C. signal from approximately 3 to 6 volts was applied by adjusting the 1 kohm potentiometer. The transfer characteristic for two devices is shown in Figure IV-45. The output is close to linear over the input range of 3.4 volts up to 5.8 volts. This information was used to establish the voltages levels used in the other four input switch positions. In addition to the transfer characteristic, the output level on a number of circuits for a fixed input level was measured. These values are illustrated in the graph in Figure IV-46. The output voltage levels range from 2.4 volts up to 3.6 volts with the largest number around 2.7 volts.

The next function in Table IV-2 is the signal V_{DD} voltage. The typical value of 12 volts was utilized for the test tool. This voltage is supplied to the drain of each of the two output transistors via pin 9.

The driver V_{DD} voltage, connected to pin 20, supplies the power to the clock generator and to the four phase clocks that go to the shift register. This was also set at 12 volts.

The signal V_{DD} current given in Table IV-2 is a typical value of 8 mA. This value is dependent upon the output load and the output voltage level. For the test tool with a 2 kohm load connected to one of the two outputs at a time, a current of 2 mA will flow when that output is not being addressed, and 1 to 2 mA will flow when it is being addressed. This corresponds to an output level of 2 to 4 volts.

The driver V_{DD} current is given as a typical value of 8 mA. This value is frequency dependent and also dependent upon the load on Ø3 out (pin 19). Using the test tool this current typically measured 13 mA.

The reset drain voltage is supplied to both the even (pin 13) and odd (pin 14) reset drain pins. The typical value of 9 volts was utilized. This voltage is supplied to the output transistor to reset the gate to its high level prior to the addition of the charge to the gate from the shift register.

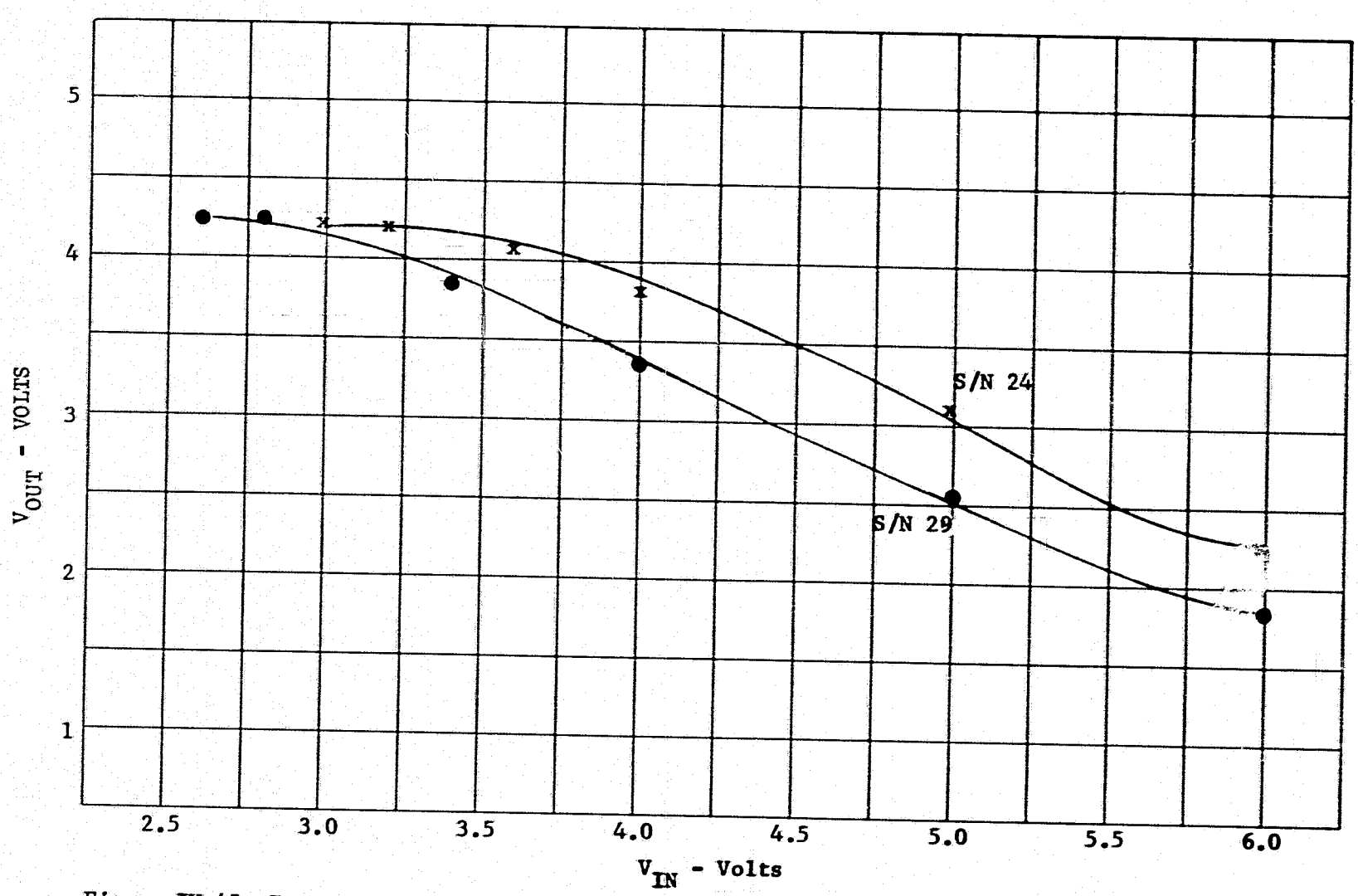


Figure IV-45 Transfer Characteristics

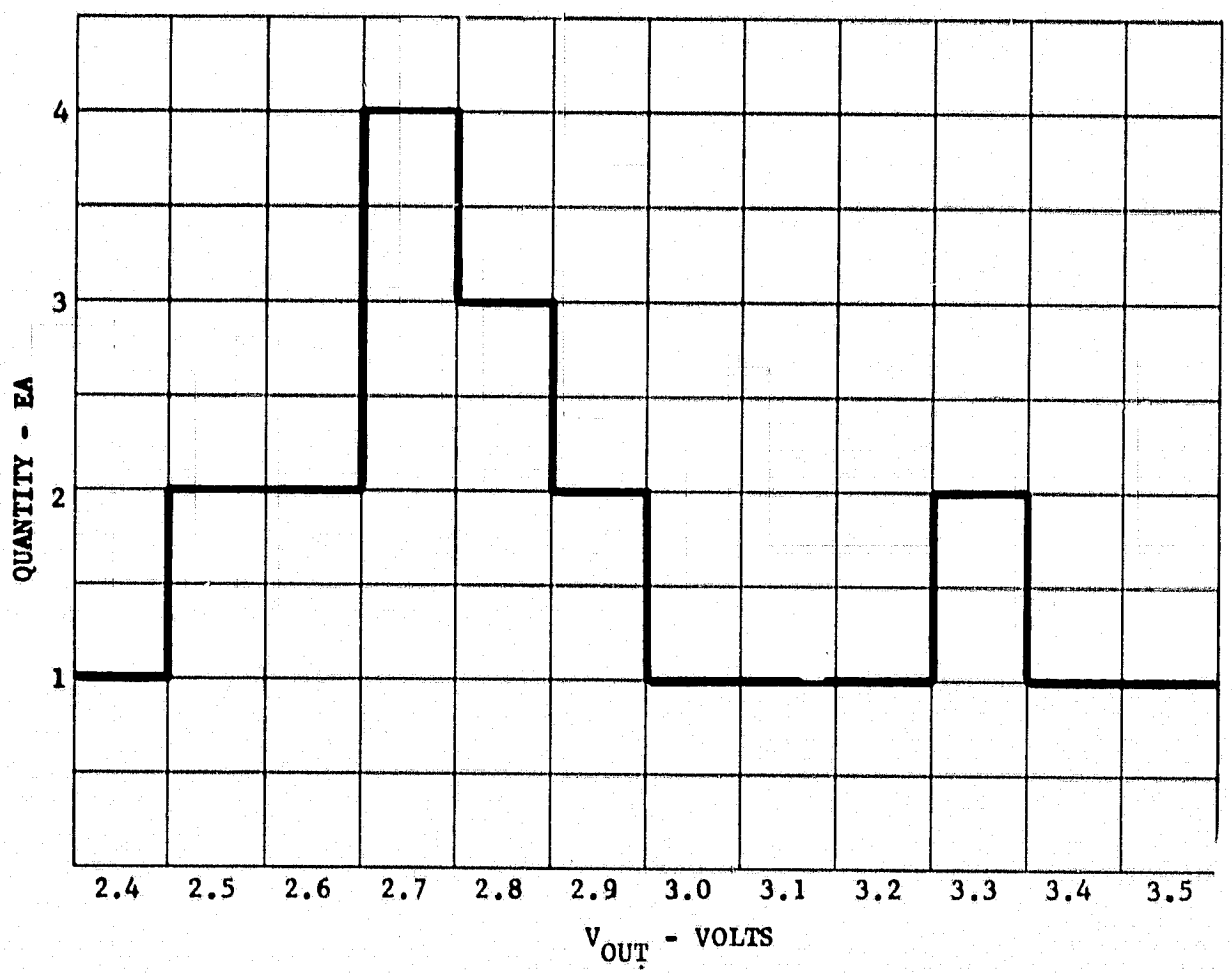


Figure IV-46 Output Levels with Fixed Input, 21 Devices

The reset drain current is listed as a typical value of 70 uA. The actual current flow is the current required to recharge the output transistor gate (Figure IV-3) following the addition of the negative charge from the channel. This current flow is an exponentially decaying function related to the output series resistance, the resistance of the series FET and the capacitance to be charged. The initial charging current on the test assuming the conditions which produce the highest possible current is on the order of 9V/100 kohm = 90 uA. The time constant for this charging current is on the order of one microsecond.

The clock output (pin 19) is a square wave output with a maximum amplitude of V_{DD}. This signal is the same phase as the $\phi 3$ clock going to the shift register. In the test tool this signal is utilized to provide the correct timing for the sample and hold to accept the output level when it is valid. In normal operation this signal can be used to generate the timing to operate several of these circuits in synchronization.

The signal outputs on this device are pins 8 and 12. The test tool utilizes the 2 kohm load specified in the data sheet. The output voltage level for a given input was shown previously in Figures IV-45 and IV-46. This output voltage with the 2 kohm load is a square wave with the reset portion being at approximately 4 volts and the signal portion ranging from 2 to 4 volts. V_{01} (pin 12) has a valid output level when $\phi 3$ is low and V_{02} (pin 8) is valid when $\phi 3$ out is high.

In addition to the pins listed in Table IV-2, the substrate (pin 1), the clock ground (pin 2), and the signal ground (pin 11) are all held at ground potential.

Table IV-3 lists the electrical measurements made on the R5101 devices. The temperatures utilized for this testing were +25°C, -25°C and +55°C. The high test temperature was selected after characterizing the circuits for their minimum operating frequency at a given temperature. In the test tool with the clock input at 125 KHz the circuits would operate up to about 40°C. To operate at 55°C a clock input of 350 KHz was required and at 85°C, 0.5-1.0 MHz was required. The minimum operating frequency is determined by thermal leakage effects on the die. Since the thermal leakage doubles every 8-10°C, the minimum operating frequency must also increase in a similar manner. The test tool was designed to operate with a clock input frequency of 125 KHz for the various electrical parameters measured. The only measurement that was adversely effected by the increased frequency necessary at 55°C was the noise measurement. This will be discussed in the electrical parameter section. The initial electrical characterization was utilized to provide in-depth information about the electrical performance of these devices. The objective of the

TABLE IV-3 ELECTRICAL TESTS, R5101

SEQUENCE	TEMPERATURE	TEST TYPE
1) INITIAL CHARACTERIZATION	25, -25 & 55°C	FULL
2) POST ENVIRONMENTAL SCREEN	25°C	INTERIM
3) POST 160 HR BURN-IN	25°C -25 & 55°C	FULL INTERIM
4) STEP STRESS	25°C	INTERIM
5) HIGH TEMP LIFE TEST @ 4, 8, 16, 32, 64, 128, 256, 500, 1000 & 2000 HOURS	25°C	INTERIM
6) POST HIGH TEMP LIFE TEST	25°C	FULL
7) TEMPERATURE CYCLING @ 20, 50, 250, 500 & 1000 CYCLES	25°C	INTERIM

NOTE: Interim electricals = Reset Drain Current, Clock Current, Gain, Signal Current, Offset Voltage and Input Leakage Current.

Full electricals = Interim Electricals plus - Noise, Bandwidth and Transfer Efficiency.

post environmental characterization tests was to determine delta shift information on each device. The interim electrical tests were used to assure that the devices were functional at the specified points in the test and also to obtain additional parameteric data for delta shift analysis.

2. Electrical Parameter Measurements

a. Device Power - Two current levels were measured for the R5101. These were the current drawn by the clock circuitry and the current drawn by the output transistor. Both of these currents were measured on the test tool by reading the voltage drop across a 14.7 ohm resistor and calculating the current flow. A typical value for the clock current reading was 0.1991 volts which calculates out as 13 mA. A typical value for the output signal current reading was .0250 volts which corresponds to 1.7 mA. The data was taken on an HP9830 computer and stored on cassette tape. Shift in these current levels would indicate possible threshold voltage drift, shorting between the polysilicon layers, or shorts from the polysilicon up to the overlying metallization or down to the silicon.

b. Input Gate Leakage - Input gate leakage is measured on the test tool for the reset drain current. This is measured across the 100K current limiting resistor as shown. This test is utilized to indicate an increase in the leakage current on the output transistor gate and is not designed to measure the momentary charging currents. A voltage mesurement of 1 volt would indicate a current leakage of 10 uA. The remainder of the gates are measured on the leakage current test tool shown in Figure IV-47. The inputs measured were V_{IG}, V_I, Sync, Cp, and V_{OG}. A constant 11 volts is applied to each of these inputs through a 100 kohm limiting resistor. The voltage is then measured across each of these resistors and recorded. Resolution down to .0001 volts was utilized which provided a current sensitivity of 1 nanoamp. Another leakage current which could be measured on this type of part with more than one polysilicon conductive layer is the leakage between overlapping layers. For CCD analog delay lines this would commonly include gates in the input and output sections and on devices without an on-circuit clock generator this would include the transfer electrodes. For the R5101 the input V_{IG} to V_I leakage should have been measured. The probable parametric result of this type of leakage would be a shift in the transfer characteristic. The significance of this type of measurement will be move evident in the section on the CCD321A-2.

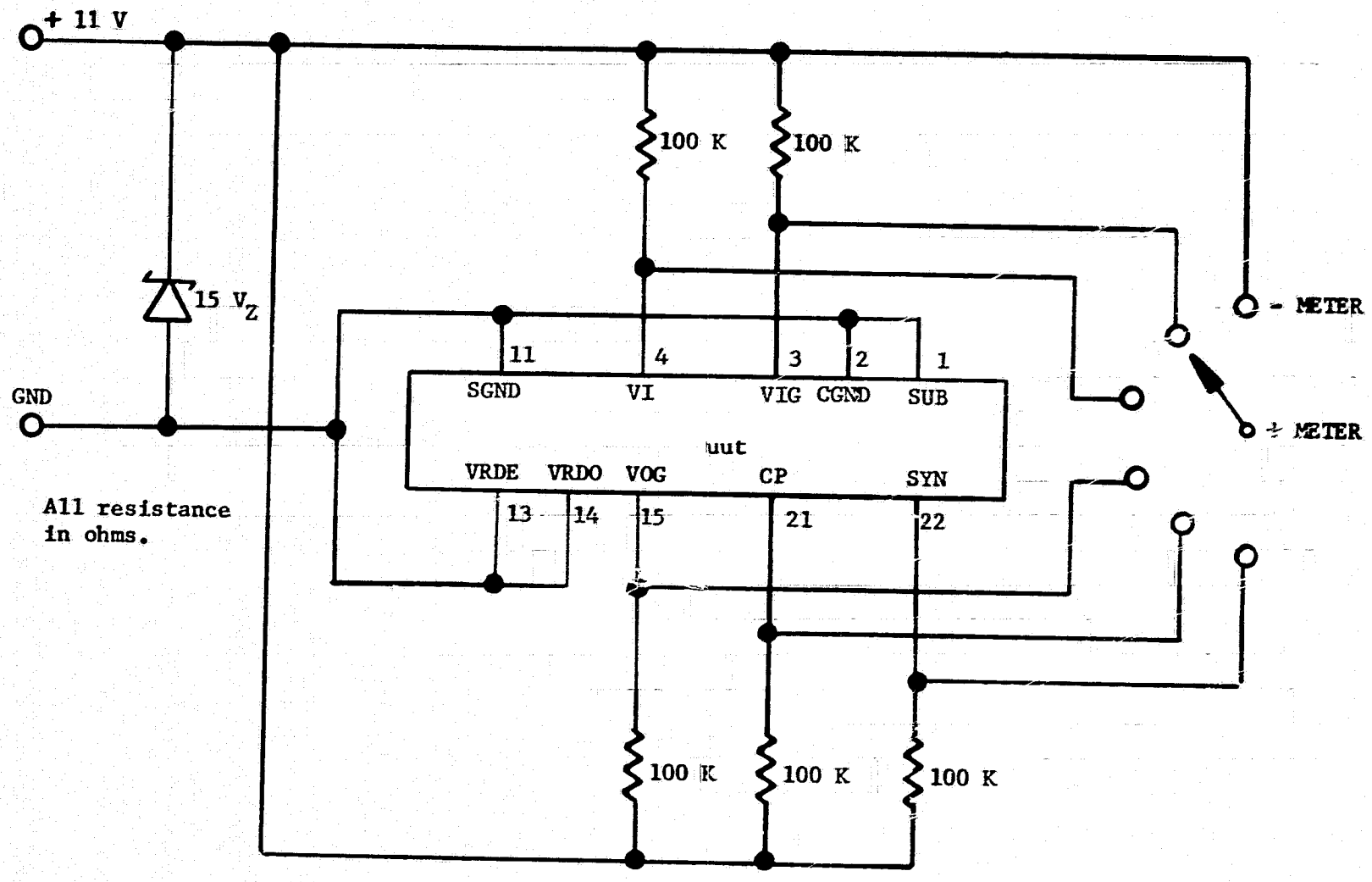


Figure IV-47 Schematic, Leakage Test Tool, R5101

c. Voltage Offset - This term describes the current that is thermally generated within the bulk silicon. With no charge input into the device the output voltage level will approach that of the reset level. In the test tool the input is taken to ground which eliminates any charge input. As can be seen in the transfer characteristic in Figure IV-45 the output does not change for inputs below about 3 volts. This thermally generated current increases with temperature and this is evident in the electrical measurements. A direct comparison can be made between the -25 °C and +25 °C readings since they were performed at the same operating frequency. A typical device measured a V offset level of 4.01 volts at 25 °C and a level of 4.24 volts at -25 °C. The increased frequency of operation at 55°C produced an offset voltage level of 3.87 volts. A more accurate measurement of the offset level and one that would eliminate temperature related changes in the output amplifier operating point would require two readings for this measurement. This would require the voltage reset level to be measured followed by the output level with no charge being transported. Subtracting the second from the first would provide the voltage level related to thermally generated charge.

d. Voltage Gain = The voltage gain is performed by measuring the output voltage level change for a known change in the input voltage level. In the test tool, readings were taken with the input switched to position 5 (5V) and then with the input switched to position 4 (4V). The second output level substracted from the first, divided by 1 volt is equal to the gain. A change in the gain would indicate a shift in the input sensitivity, the transfer efficiency, or the output amplifier gain. The input voltage levels were selected by utilizing the characterization data shown in Figure IV-45. The input levels were selected within the linear portion of the curve.

e. Noise Measurement - CCD noise is partially a function of the magnitude of the dark current. It is also affected by input circuit charging noise, reset circuit charging noise, output amplifier noise, and surface and bulk state trapping noise along the CCD shift register. Poor process controls and poor grade material can seriously affect the noise properties of CCDs. To take the noise measurement on the test tool the input was put in position 5, switch 6 was connected to U6-8, and switch 7 was connected to U8-6. The first sample and hold circuit would acquire the output level at a valid portion of this signal. The signal is sampled at the time when U15-8

goes low with a sample time of 8 microseconds. The 5,000 pF holding capacitor provides accuracy to 0.1% in 6 microseconds on U9. The second sample and hold, U10, is held in the sample position starting at the same time as U9 and remaining for 640 microseconds. With the 0.15 uF capacitor this circuit will reach 0.1% accuracy in 700 us. With the higher value capacitor the drift on the output is only 0.06 mV per second. These two sample and hold circuits in series provide the necessary fast sampling time as well as the slow output level drift to read individual voltage levels on the R5101 outputs. In this circuit configuration a new sample is read every 33 milliseconds while the computer accepts a sample every 250 milliseconds. To obtain an rms voltage reading, 125 samples are accepted and this value calculated.

$$(\text{RMS noise})^2 = \sum_{i=1}^{125} (x_i - \bar{x})^2$$

There were three problems associated with taking this measurement. The first one was the system noise since there were several A.C. signals in the test tool. This could result in erroneous readings being taken by the computer. The second problem was the change in the output voltage level as the chip heated up while operating. The output voltage level versus time is shown in Figure IV-48. With this device in the test tool for 200 seconds the output level went from 1.7268 volts to 1.6998 volts. This is a change of 27 mV. This is one of the larger changes seen, however, it illustrates the problem. The third problem only affected the high temperature reading. Since the holding capacitors on the test tool were adjusted for proper operation at a clock frequency of 125 KHz, they were not optimized for the higher operating frequency. There would also be an increase in system noise at the higher frequency.

f. Bandwidth - The test tool was utilized for this test on the R5101. The switches were connected to the bandwidth positions as shown on the schematic. The DC voltage to pin 4 was set at 4.5 volts and an AC signal of 2 volts peak to peak was applied through the capacitor to the device. The clock pulse used was 2 MHz which is the maximum specified in the data sheet. The procedure used was first to measure the output peak to peak voltage level at 10 KHz to establish the device gain. The input sine wave frequency was then increased while the output level was monitored. When the signal had dropped off 3db from the starting point the input signal frequency was read and recorded. These devices typically had bandwidths that ranged from about 140 to 180 KHz with the exception of the circuits which were later identified to

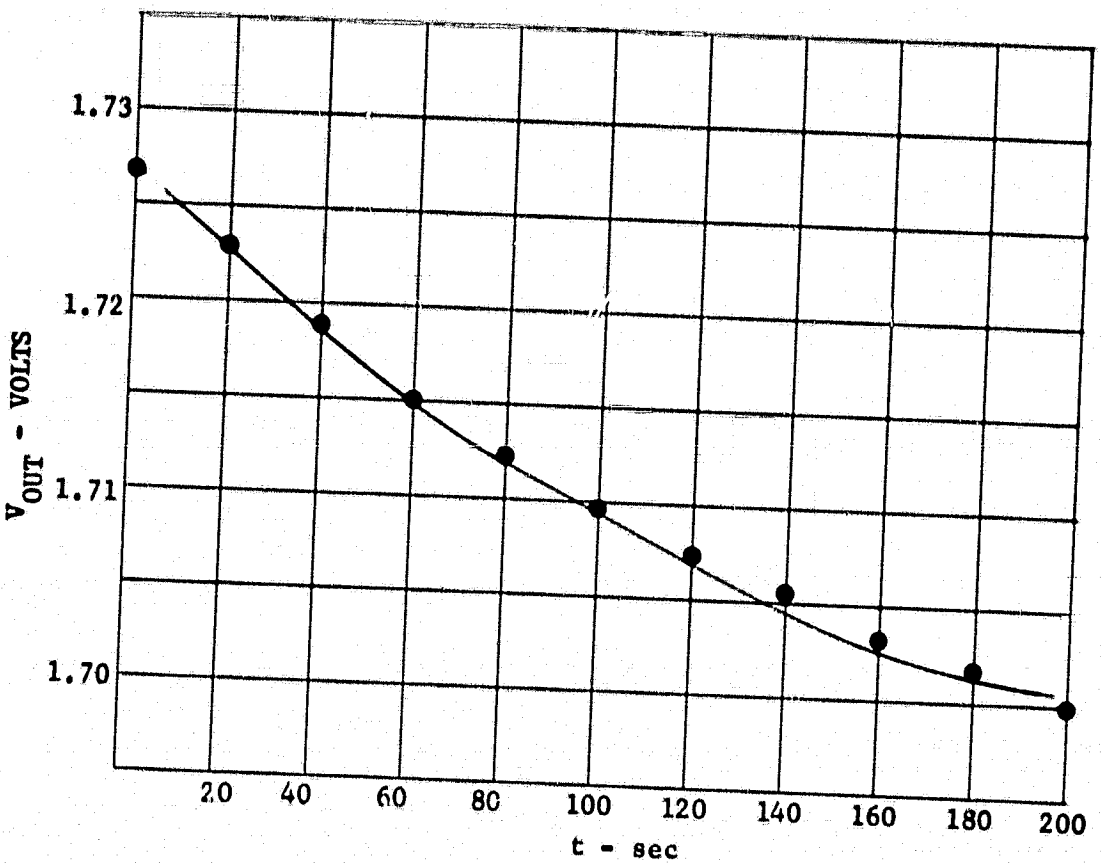


Figure IV-48 Output Level vs Warmup Time

have shorts within the clock circuitry. These devices had significantly lower bandwidths and often had distorted output signals i.e., nonlinear gain or decreased input signal range.

g. Transfer Efficiency - This is one of the fundamental parameters for CCDs since it is a measure of several first and second order processing and material effects. These are, in part:

1) Shift register gate overlap completeness;

2) Charge trapping losses;

3) Well discontinuity along the shift register;

4) Inconsistencies in the work function of the polysilicon gate structure.

This measurement is made by shifting a charge packet through the device and measuring the output voltage (V1) then switching to no charge being transferred through and measuring this voltage level (V2) and finally measuring the voltage level (V3) which occurs at the single pulse following the change from V1 to V2. The transfer efficiency is then equal to:

$$1 - \left[\frac{V2 - V3}{V1 \times \text{no. of tranfers}}\right]$$

The test tool circuitry was designed to perform these measurements. Switches 8 and 9 control the input levels, and the counter circuits, U11, U12, and U13 control the sample time for the sample and hold circuits to read the voltage levels. The critical timing for this test is to read the voltage level (V3) which occurs at the single output pulse following the change from charge being transferred through to no charge being transferred through. In the test tool with switch 9 at ground and switch 8 at 5 volts the input to the R5101 is 5 volts DC. This provides the output level V1 of about 2.7 volts. To measure V2, with no charge being transferred through, 3 volts dc is applied to the R5101 with both switches 8 and 9 at 5 volts. This provides an output level of approximately 4 volts. The V3 measurement is taken by having switch 9 at 5 volts and switch 8 going to U3-3. In this configuration the input to the R5101 is switching between the 3 volt input level and the 5 volt input level. When the input switches from 5 volts to 3 volts the counters reset and count to 2000, since this is a 2000 stage delay line. The counter circuitry then provides a pulse that is used to control the timing for

the sample and hold circuit to take the correct voltage reading. The R5101 output is shown in Figure IV-49. This is 0.5 volts per vertical division and 2ms per horizontal division. The rising edge of this output is then expanded in Figure IV-50. The sample and hold control pulse is also shown in Figure IV-50. The top trace is at 5 volts per vertical division and the bottom trace is again at 0.5 volts per vertical division. The timing is 20 microseconds per horizontal division.

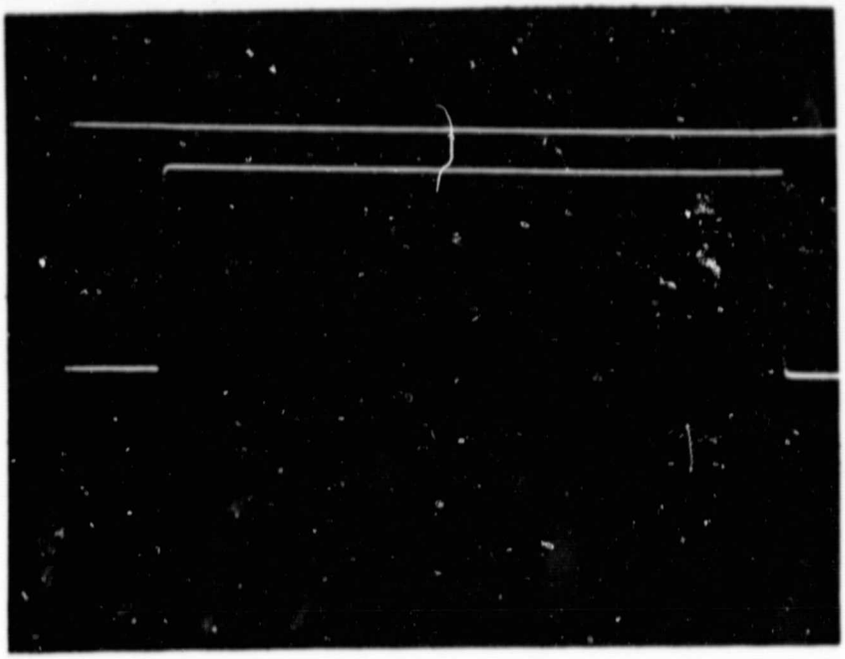


Figure IV-49 Output Voltage, 0.5 V/cm Vert., 2 ms/cm Horiz., R5101

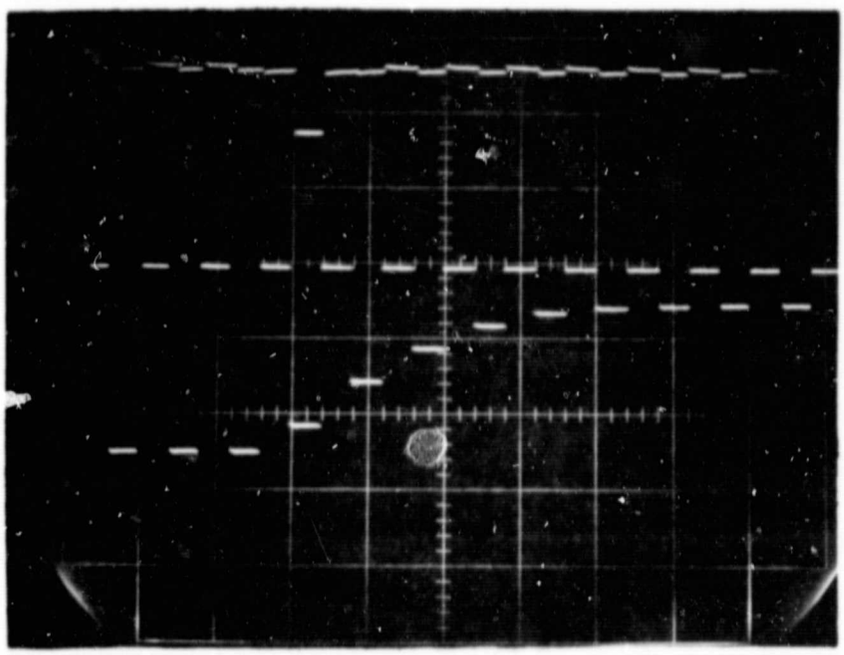


Figure IV-50 Output Voltage and Sample & Hold Enable Pulse, 20 u seconds/cm Time Base, R5101

The top trace remains at 5 volts except for the single low which inputs V3 to the sample and hold circuit. The bottom trace is of the circuit output. The upper level on the square wave is the reset voltage level between valid output times. This is about 4.2 volts. The voltage level on the left hand side of the picture is V1 and the voltage level on the far right hand side of the picture is V2, These are about 2.7 and 4.0 volts respectively.

The value of V3 which is read by the sample and hold is about 2.9 volts. As can be seen in the photograph the transfer efficiency cannot be calculated by using these three values alone since there is additional charge being transferred out over the next 5 or 6 pulses. This value was used to track any changes in the transfer efficiency during the course of this test. This provides a sensitive parameter for following these changes.

To calculate the actual transfer efficiency for this device the total amount of charge has to be accounted for. Readings of the voltage levels were taken through the transition period shown in Figure IV-50. These readings are: V1 = 2.69, V2 = 3.99, and in between 2.91, 3.31, 3.60, 3.84, 3.97, and 3.98. Assuming a linear response of the output amplifier with charge then the transfer efficiency can be calculated in the following manner:

The inefficiency for the transfer of charge from input to output

$$= \frac{(3.99 - 3.98) + (3.99 - 3.97) + (3.99 - 3.84)}{(3.99 - 2.69) \times 2000}$$

$$+ \frac{(3.99 - 3.60) + (3.99 - 3.31) + (3.99 - 2.91)}{(3.99 - 2.69) \times 2000}$$

$$= \frac{2.33}{1.3 \times 2000} = 8.96 \times 10^{-4}$$

$$\text{efficiency} = 1 - \text{inefficiency}$$

$$= 0.999104$$

The numerator in this formula is the summation of the voltage differences at the output. The denominator is the voltage difference caused by a charge packet reaching the output multiplied by the number of times this charge is transferred. The efficiency calculated and recorded during the normal testing of this device was:

$$1 - \left[\frac{3.99 - 2.91}{2.69 \times 2000} \right] = 0.999799$$

This value is high for two reasons. The first is that the additional charge on the 5 pulses after the 2.91 was measured is neglected, and the second is the fact that the 2.69 in the denominator is not proportional to the size of the charge packet. A value of 3.99-2.69 would have been more accurate. This would have given an efficiency of:

$$1 - \left[\frac{3.99 - 2.91}{(3.99 - 2.69) \times 2000} \right] = .999585$$

This is still high but is more nearly accurate. The maximum and minimum values for transfer efficiency as calculated during this test are:

At V3 = 3.99
Transfer eff = 1.0

At V3 = 2.69
Transfer eff = .999758

C. Initial Electrical Characterization

The test flow is shown in Figure IV-51. Initial electrical characterization on the R5101 devices was performed as described in the previous section. The leakage current test found four parts with leakage (Table IV-4). S/N 5 has the sync input shorted to ground and this input is also leaky on S/N 25. The other two devices have nanoamp level leakage currents.

All fifty devices were electrically characterized at -25°C, +25°C, and +55°C. A sample of the electrical readings are given in Table IV-5. This provides the data taken on the test tool at the three temperatures. The effect of temperature on these devices appears to vary significantly. As an example, the offset voltage on serial number 1 is the same at -25°C and +25°C and decreases by 0.15 volts at +55°C. Serial number 3 decreases by 0.25 volts between -25°C and +25°C, and decreases by 0.42 volts between +25°C, and +55°C. Other parameters also were affected to varying amounts by temperature on the different parts. Delta calculations between these initial measurements and later measurements will be discussed in the data analysis section.

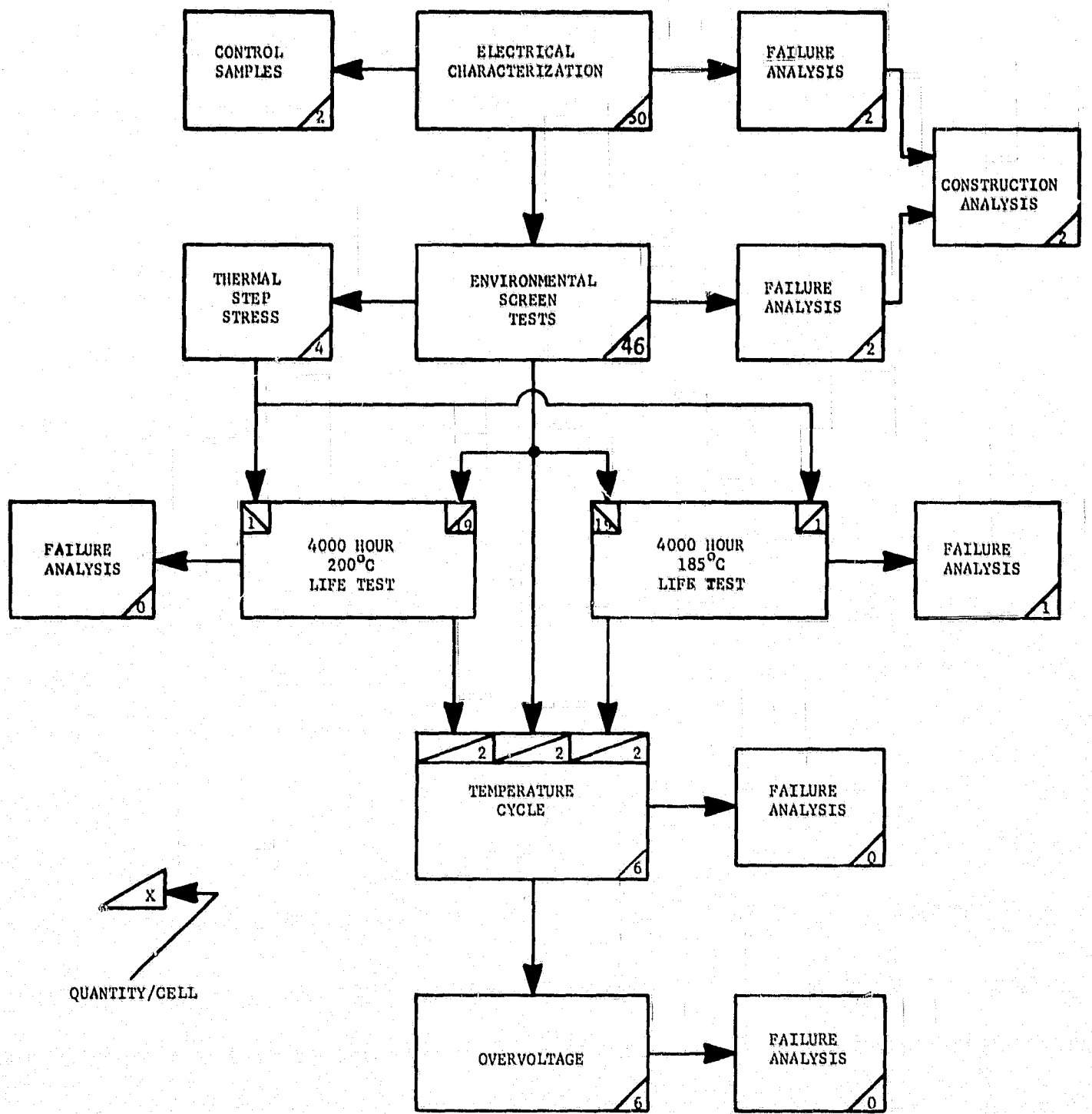


Figure IV-51 Test Flow Diagram, Reticon R5101/ Quantities Used

TABLE IV-4 LEAKAGE TEST, INITIAL @ 25°C, R5101

SERIAL NUMBER	PIN	CURRENT
5	22	109 nA
13	15	92 nA
25	22	1.5 uA
33	15	386 nA
33	3, 4 21, 22	2 nA

Table IV-5 Initial Electrical Characterization, R5101

Parameter	Test Conditions		Spec. Limits Typical[2]	Units	Serial Number 1	3	5
Driver Current	Note 1	-25°C	8	mA	13.31	14.51	14.43
		+25°C			13.26	13.20	12.91
		+55°C			15.69	15.05	14.93
Signal Current	Note 1	-25°C	8	mA	1.74	1.81	1.73
		+25°C			1.71	1.66	1.56
		+55°C			1.69	1.53	1.56
Offset Voltage	Note 1 V_{IN} = 0.0 V	-25°C	-	V	4.06	4.14	4.08
		+25°C			4.06	3.89	3.83
		+55°C			3.91	3.47	3.68
Gain Side 1	Note 1 Delta V_{IN} = 1.0 V	-25°C	0.6	V/V	.82	.81	.88
		+25°C			.82	.66	.76
		+55°C			.76	.58	.73
Gain Side 2	Note 1 Delta V_{IN} = 1.0 V	-25°C	0.6	V/V	.84	.84	.90
		+25°C			.84	.67	.77
		+55°C			.79	.58	.74
Noise Side 1	Note 1 V_{IN} = 5.0 V	-25°C	-	mV	.47	.53	.55
		+25°C			.56	.48	.46
		+55°C			8.40	9.85	10.24
Noise Side 2	Note 1 V_{IN} = 5.0 V	-25°C	-	mV	.52	.60	.62
		+25°C			.64	.72	.55
		+55°C			1.86	3.45	2.41
Transfer Eff. Side 1	Note 1	-25°C	-		.999614	.999669	.999661
		+25°C			.999616	.999687	.999658
		+55°C			.999630	.999636	.999676
Transfer Eff. Side 2	Note 1	-25°C	-		.999607	.999660	.999653
		+25°C			.999608	.999685	.999656
		+55°C			.999634	.999648	.999686

Note 1 - V_{DD}=12 V, Ø3 out load = 1.5 kohm, V01 and V02 load = 2 kohm, sampling frequency = 62.5 KHz at -25°C and +25°C, 175 KHz at +55°C.

Note 2 - No maximum and minimum specifications available.

Table IV-6 provides the clock current measurements at 25°C for each of the devices. The serial numbers which had low bandwidth or high leakage currents are also indicated. All of the devices with high clock current had low bandwidth or distorted output signals. These devices were later analyzed and will be discussed in the failure analysis section. The bandwidth readings for each of the fifty devices at all three temperatures are given in Table IV-7.

Serial numbers 5 and 25 were removed from test and held for failure analysis. These were the two devices with input leakage on pin 22. Serial numbers 1 and 2 were held for control samples. These samples are tested and recorded before each electrical test on the remaining devices.

D. Environmental Screen

Forty-six devices were subjected to the environmental screening tests of Table IV-8. These tests were selected from MIL-STD-883, Method 5004, Class B. Internal visual was not implemented at this point since parts will be examined for the construction analysis and during the failure analysis.

The first screen test was high-temperature storage per Method 1008.1, Condition C. This is an storage temperature of 150°C for 24 hours in a nonpowered condition. This stress is used in the screening sequence as a pre-conditioning treatment prior to the remaining tests.

The second environmental screen test was temperature cycling per Method 1010.2. This is an automated test which exposes the parts to -65°C and +150°C taking 30 minutes per temperature cycle. There was a total of 10 cycles.

The third screen test was constant acceleration per Method 2001.2, Condition E. This is a 30,000 g acceleration in the Y1 axis. The Y1 orientation is defined as that one in which the element tends to be removed from its mount. The parts were held in plastic carriers to avoid bending of the external leads.

The fourth screen test is a seal test per Method 1014.2. The fine leak test is per test condition A1, using helium tracer gas with a bomb time of 2 hours at 60 PSIG. The gross leak test is per Test Condition C, using fluorocarbon.

Interim electrical tests were performed at this point. These tests are used to verify the functionality of the devices and provide information on the effect of the preceding tests on parameter stability. These data were stored on tape and delta calculations performed. The gain of S/N 23 side 1 was found to have shifted by 17%. This part was left in test to see if any further change would occur.

TABLE IV-6 INITIAL CLOCK CURRENT AT 25°C, R5101

S/N	CLOCK CURRENT mA	S/N	CLOCK CURRENT mA	S/N	CLOCK CURRENT mA	S/N	CLOCK CURRENT mA
1	13.26	13*	29.53	26	12.91	39*	29.47
2	12.84	14	13.06	27*	12.84	40	13.45
3	13.20	15	13.18	28	13.51	41	12.91
4	12.84	16*	13.04	29	13.11	42*	33.45
5*▲	12.91	17	12.77	30	12.97	43	13.24
6	13.65	18	13.45	31	13.15	44	12.57
7*	30.61	19	12.77	32	13.18	45*	13.92
8	12.97	20	13.31	33	12.70	46	13.31
9	12.77	21	13.04	34	13.24	47	13.65
10	12.84	22*	36.42	35	12.76	48	13.72
11	13.11	23	12.49	36	12.98	49	12.65
12	13.24	24	13.31	37*	21.28	50	14.05
		25*▲	13.24	38*	33.48		

* Low Bandwidth ▲ High Leakage

TABLE IV-7a BANDWIDTH (KHz) @ -25°C; R5101

S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2
1	170	180	13	*200	210	26	170	150	39	*150	140
2	200	210	14	180	180	27	80	80	40	150	150
3	180	180	15	170	190	28	150	140	41	160	170
4	170	170	16	90	90	29	160	150	42	*100	100
5	90	90	17	170	170	30	170	180	43	150	160
6	170	170	18	170	170	31	150	160	44	140	140
7	*100	100	19	160	160	32	170	170	45	90	90
8	180	180	20	150	150	33	170	170	46	150	160
9	180	170	21	170	180	34	160	160	47	150	170
10	170	170	22	*100	110	35	160	150	48	100	100
11	130	130	23	160	140	36	160	160	49	170	180
12	170	170	24	140	130	37	100	110	50	160	160
			25	100	100	38	*100	110			

* DISTORTED WAVEFORM

TABLE IV-7b BANDWIDTH (KHz) @ 25°C; R5101

S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2
1	160	150	13	*150	170	26	170	160	39	*130	140
2	150	160	14	180	180	27	80	80	40	170	160
3	130	120	15	170	180	28	160	150	41	150	170
4	160	140	16	90	90	29	160	160	42	*100	100
5	80	80	17	170	170	30	160	170	43	150	170
6	170	170	18	170	170	31	160	170	44	140	140
7	*100	100	19	160	170	32	180	180	45	90	90
8	140	150	20	150	150	33	170	170	46	180	170
9	160	170	21	160	180	34	160	170	47	150	170
10	170	170	22	*70	90	35	180	180	48	100	100
11	130	140	23	130	140	36	160	160	49	160	160
12	150	170	24	150	150	37	100	100	50	160	160
			25	100	100	38	*100	100			

* DISTORTED WAVEFORM

TABLE IV-7c BANDWIDTH (KHz) @ 55°C; R5101

S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2	S/N	VO1	VO2
1	150	180	13	*120	150	26	160	170	39	*120	130
2	190	190	14	180	180	27	80	80	40	160	160
3	170	170	15	180	190	28	160	160	41	160	150
4	170	180	16	90	90	29	170	180	42	*100	100
5	80	90	17	170	180	30	150	150	43	160	160
6	170	180	18	170	170	31	150	170	44	140	140
7	*110	110	19	170	170	32	170	180	45	90	90
8	170	180	20	160	160	33	160	170	46	170	190
9	170	170	21	170	180	34	180	190	47	160	180
10	170	170	22	*100	100	35	180	190	48	110	110
11	130	130	23	150	150	36	160	160	49	170	170
12	170	180	24	150	160	37	100	110	50	170	190
			25	100	110	38	*90	110			

* DISTORTED WAVEFORM

TABLE IV-8 SCREENING REQUIREMENTS (MIL-STD-883)

SCREEN TEST	METHOD	REMARKS
1. INTERNAL VISUAL	--	N/A, COMMERCIAL PARTS. CONSTRUCTION ANALYSIS WILL BE PERFORMED.
2. SERIALIZATION	--	
3. STABILIZATION BAKE	METHOD 1008, 24 HOURS MIN TEST CONDITION C	150°C
4. TEMPERATURE CYCLING	METHOD 1010	-65 to 150°C
5. CONSTANT ACCELERATION	METHOD 2001	30,000 G, Y_1 AXIS ONLY
6. SEAL		
a) FINE	METHOD 1014	TEST CONDITION A, TRACER GAS HELIUM
b) GROSS	METHOD 1014	TEST CONDITION C, FLUOROCARBON
7. INTERIM (PRE BURN-IN) ELECTRICAL PARAMETERS	--	25°C
8. BURN-IN	METHOD 1015	TEST TEMPERATURE 55°C, 160 HOURS
9. FINAL ELECTRICAL 1) 25°C 2) -25°C 3) 55°C	--	THESE ELECTRICAL TESTS ARE TO BE COMBINED WITH THE FIRST ELECTRICAL TESTS FOR THE HIGH TEMPERATURE LIFE TEST.
10. EXTERNAL VISUAL	METHOD 2009	

The fifth screening test was the burn-in per Method 1015.2. The temperature was lowered from the specified 125°C to 55°C. This is the maximum test temperature used on these devices and the higher temperature effects were not known until the thermal step stress portion of the test was performed.

Following this 160 hour burn-in the parts were again electrically characterized. S/N 23 had again shifted. The gain values on Side 1 for the three electrical tests were 0.5606, .6551, and .5830. One additional device, S/N 31 had a significant increase in clock current. This device went from 14 mA to 34 mA. There two devices were pulled from test and held for failure analysis. They will be discussed in that section.

E. Thermal Step Stress Test

This test was performed to establish the temperatures to be used in the 4000 hour life test. The circuit used is the same one as that to be used for the life test. The test plan followed was:

1. Operate four circuits for 16 hours at +65°C. Monitor the outputs for functionality and also record the power supply currents at the start and end of test.

2. Perform the interim electrical tests at +25°C.

3. Increase the operating temperautre in 10 °C increments and repeat the 16 hour operating test and interim electricals.

4. Continue 10 °C increments until malfunction or permanent parameter shift occurs. Malfunction is defined as the point where the output, which has previously reached saturation, no longer exhibits a regular time sampled analog pulse train. Other malfunction criteria is any significant shift in current at temperature.

   As mentioned the output will reach saturation. This occurs because the register dark signal doubles every 8 to 10 degrees centigrade. The circuit will operate normally with a saturated output signal except that input signal control is lost. The current flows on each of the 5 power supplies was monitored at the start and end of each 16 hour period. There was no change on any of the power supplies during the course of the test except for the +12 volt line that supplied both the clock current and the signal current to the R5101. The variation in this current level with temperature is shown in Table IV-9. The current increased up to about 95°C and then decreases above that temperature. There is a large decrease between 185°C and 195°C. The appearance of the output over the temperature range of interest is shown in Figures IV-52 through IV-57. The small white bar in the lower left hand corner indicates the ground level. These photographs are all taken with a vertical scale of 1 volt per centimeter and 100 microseconds per centimeter time base.

Table IV-9 12 Volt power supply current flow, R5101

Current flow (mA)	Temp.
75	65°C
85	75°C
95	85°C
100	95°C
90	105°C
68	115°C
66	125°C
64	135°C
62	145°C
62	155°C
61	165°C
61	175°C
58	185°C
51	195°C
47	205°C
46	215°C
45	225°C

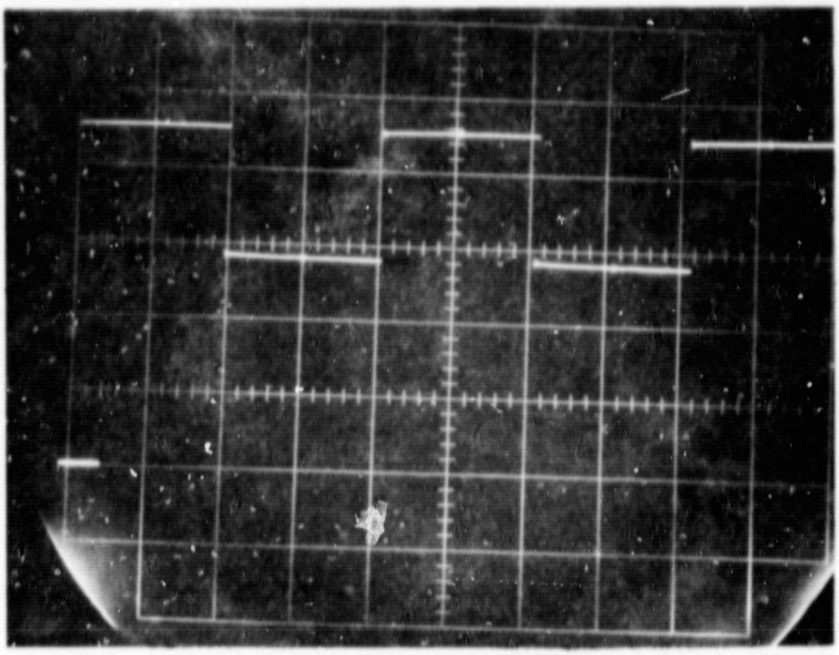


Figure IV-52 Output at 25°C, R5101

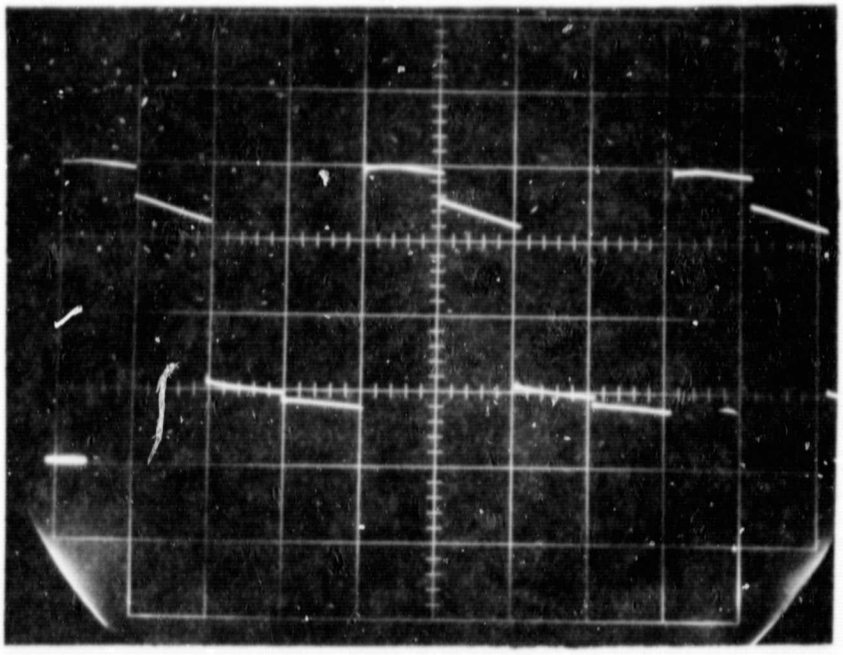


Figure IV-53 Output at 125°C, R5101

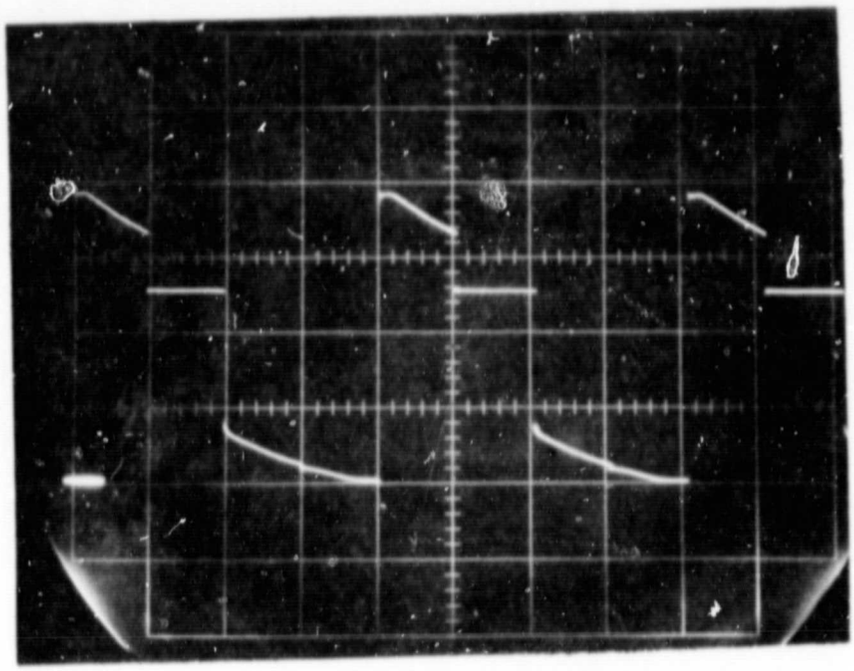


Figure IV-54 Output Waveform at 150°C, R5101

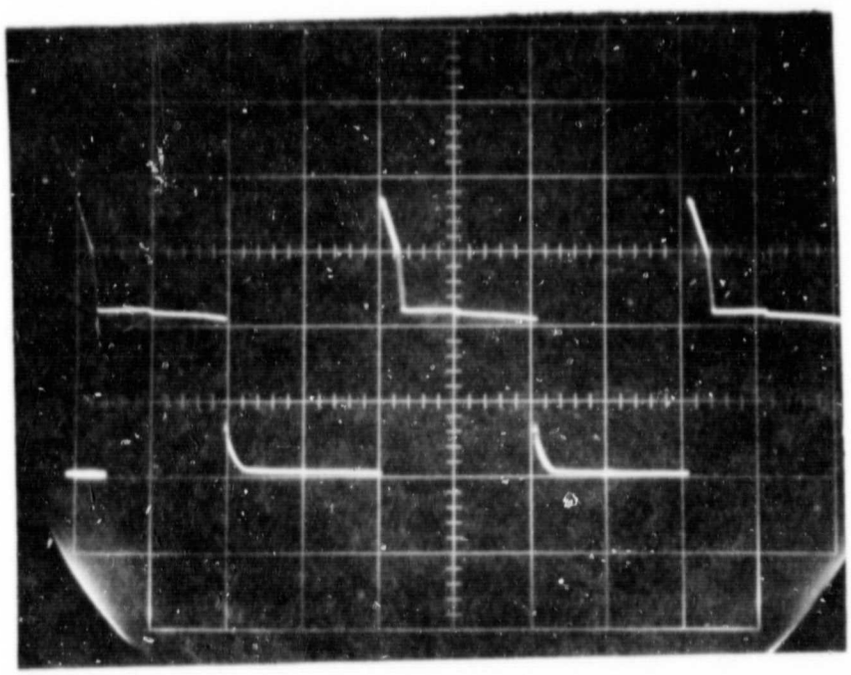


Figure IV-55 Output Waveform at 170°C, R5101

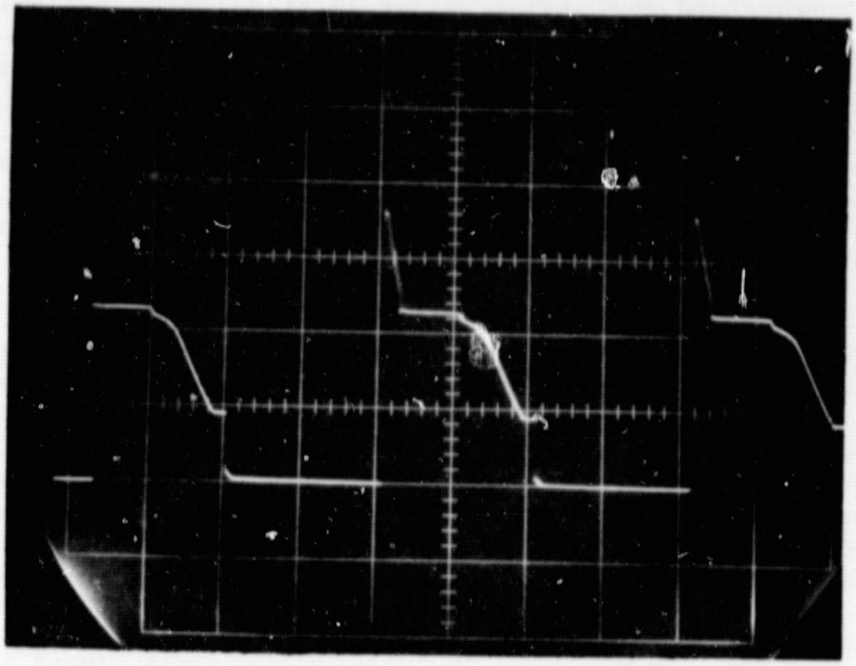


Figure IV-56 Output Waveform at 185°C, R5101

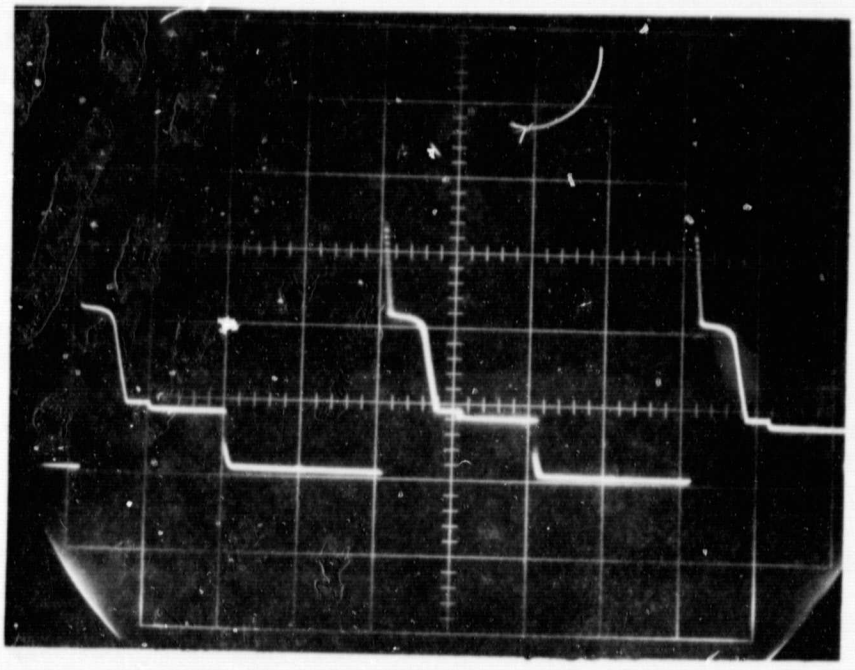


Figure IV-57 Output Waveform at 200°C, R5101

C-2

The output shown in Figure IV-52 illustrates the normal room temperature characteristic. The reset voltage level is about 4.5 volts and the analog output level is about 2.8 volts. At 125°C the output has changed to that shown in Figure IV-53. The clock pulse input is at twice the frequency of this output pulse and the influence of it can be seen at 125°C. Both voltage levels have moved downward at this point. In Figure IV-54 the output characteristic at 150°C is shown. The second half of the reset level has flattened out at about 2.6 volts and the first half of this level is slanting down toward that value.

The analog output is moving closer to ground potential. At 170°C in Figure IV-55 the first half of the reset level has almost reached the value equal to the second half. The analog signal is almost completely at ground. At 185°C the reset level is again moving from one discrete level to the next level (Figure IV-56). The change in the waveshape appearance is very similar to that which occurred between 125°C and 150°C. When the temperature is further increased to 200°C in Figure IV-57 the reset level is approaching about 0.8 volts.

The interim electrical readings taken after each 10 °C increase in temperature are shown in Table IV-10. Serial numbers 43 and 44 exhibited erratic electrical characteristics in the 155°C to 195°C range. From these erratic electrical characteristics, the drop in clock current between 185°C and 195°C, and the reduction in the output amplitude above 180°C the life test temperatures were selected. The temperatures were to be kept as high as practical so that enough failures would occur to obtain an activation energy and mean time to failure information. The upper temperature selected was 185°C and the lower temperature selected was 170°C. The parts next went into the high temperature 4000 hour life test.

F. High Temperature Life Test

The burn-in circuit used for the life test is shown in Figure IV-58. The voltages applied to the device are as shown. The clock input, pin 21, receives a 6 volt square wave pulse at 5 KHz. The clock monitor and the monitor on the remainder of the lines, allows measurement of the signals which are reaching the devices under test. If a part failure occurs this should be evident by a change in the signal at one or more of these points. The nominal 3 volts is applied to V_{IG}, V_{CB}, and V_{OG} through a 10 kohm current limiting resistor. A 5 volt Zener is attached to the leads going to the devices under test to avoid an inadvertant electrical overstress. The analog input, V_I, can have a voltage level from 3 to 6 volts applied to it. Five volts was selected since this voltage is the supply voltage for the digital circuitry and it also produces an output which can easily be observed to verify functionality of the parts in the burn-in circuit. Again a current

Table IV-10a Step Stress Electricals, S/N 41, R5101

Drain Current (nA)	Clock Current (mA)	Signal Current (mA)	Offset Voltage (V)	Gain (V/V) Side 1	Gain (V/V) Side 2		Stress Temperature (°C)	
71	13.01	1.78	4.10	.82	.85		65	
71	12.93	1.77	4.07	.81	.83		75	
71	12.95	1.78	4.09	.81	.84		85	
70	12.95	1.78	4.10	.82	.85		95	
69	12.94	1.78	4.08	.87	.89		105	
68	12.90	1.78	4.07	.81	.84		115	
68	13.36	1.85	4.20	.83	.84		125	
60	12.84	1.76	4.08	.79	.83		135	
60	12.89	1.76	4.10	.79	.83		145	
60	12.90	1.80	4.14	.83	.86		155	
60	12.77	1.76	4.08	.81	.85		165	
66	14.06	2.02	4.24	.82	.84		175	
62	12.84	1.83	4.11	.79	.82		185	
64	12.87	1.80	4.07	.81	.84		195	
65	12.92	1.81	4.10	.82	.86		205	
68	12.93	1.78	4.07	.81	.84		215	
71	12,97	1.79	4.10	.82	.85		225	

Table IV-10b Step Stress Electricals, S/N 42, R5101

Drain Current (nA)	Clock Current (mA)	Signal Current (mA)	Offset Voltage (V)	Gain (V/V) Side 1	Gain (V/V) Side 2		Stress Temperature (°C)	
89	33.82	1.65	4.00	.78	.80		65	
90	34.11	1.65	4.01	.78	.80		75	
90	34.19	1.65	4.03	.79	.81		85	
93	34.18	1.67	4.03	.79	.81		95	
91	35.70	1.75	4.17	.85	.85		105	
89	34.15	1.66	4.01	.79	.80		115	
80	33.45	1.62	3.99	.76	.78		125	
80	33.92	1.62	4.02	.77	.79		135	
80	34.67	1.65	4.14	.80	.78		145	
80	33.99	1.62	4.02	.79	.81		155	
80	33.78	1.62	4.01	.78	.80		165	
93	36.41	2.09	4.26	.87	.77		175	
86	32.22	1.68	4.05	.76	.80		185	
87	34.14	1.67	4.01	.78	.80		195	
89	34.47	1.67	4.05	.79	.81		205	
90	34.19	1.65	4.02	.78	.80		215	
91	34.19	1.66	4.04	.78	.80		225	

Table IV-10c Step Stress Electricals, S/N 43, R5101

Drain Current (nA)	Clock Current (mA)	Signal Current (mA)	Offset Voltage (V)	Gain (V/V) Side 1	Gain (V/V) Side 2		Stress Temperature (°C)	
60	13.36	1.85	4.17	.87	.88		65	
66	13.33	1.85	4.17	.86	.88		75	
58	13.38	1.87	4.19	.87	.89		85	
56	13.36	1.87	4.19	.88	.90		95	
59	13.95	1.95	4.33	.86	.90		105	
56	13.33	1.86	4.16	.87	.89		115	
50	13.78	1.88	4.24	.83	.88		125	
50	13.29	1.89	4.19	.85	.87		135	
50	13.41	1.89	4.21	.86	.87		145	
50	13.24	1.89	4.18	.87	.89		155	
50	13.24	1.89	4.18	.86	.91		165	
54	14 73	2.21	4.40	.85	.86		175	
49	13.22	1.91	4.20	.83	.85		185	
69	17.13	2.40	4.33	.90	.90		195	
53	13.36	1.89	4.19	.88	.90		205	
56	13.35	1.87	4.17	.87	.88		215	
60	13.38	1.86	4.19	.87	.89		225	

Table IV-10d Step Stress Electricals, S/N44, R5101

Drain Current (nA)	Clock Current (mA)	Signal Current (mA)	Offset Voltage (V)	Gain (V/V) Side 1	Gain (V/V) Side 2		Stress Temperature (°C)	
95	12.67	1.60	3.88	.81	.81		65	
95	12.66	1.60	3.87	.80	.80		75	
94	12.68	1.60	3.89	.81	.81		85	
93	12.66	1.60	3.89	.82	.82		95	
94	12.71	1.62	3.89	.81	.82		105	
94	12.64	1.60	3.87	.81	.81		115	
90	12.64	1.55	3.88	.80	.79		125	
90	12.57	1.55	3.88	.79	.80		135	
90	12.84	1.62	3.95	.81	.82		145	
220	12.36	1.49	3.92	.82	.81		155	
90	13.08	1.69	4.05	.82	.85		165	
114	16.97	2.10	4.04	.79	.83		175	
92	12.62	1.61	3.88	.82	.82		185	
119	16.18	2.05	4.13	.84	.83		195	
93	12.69	1.62	3.90	.82	.82		205	
93	12.63	1.60	3.87	.81	.81		215	
94	12.68	1.61	3.89	.81	.81		225	

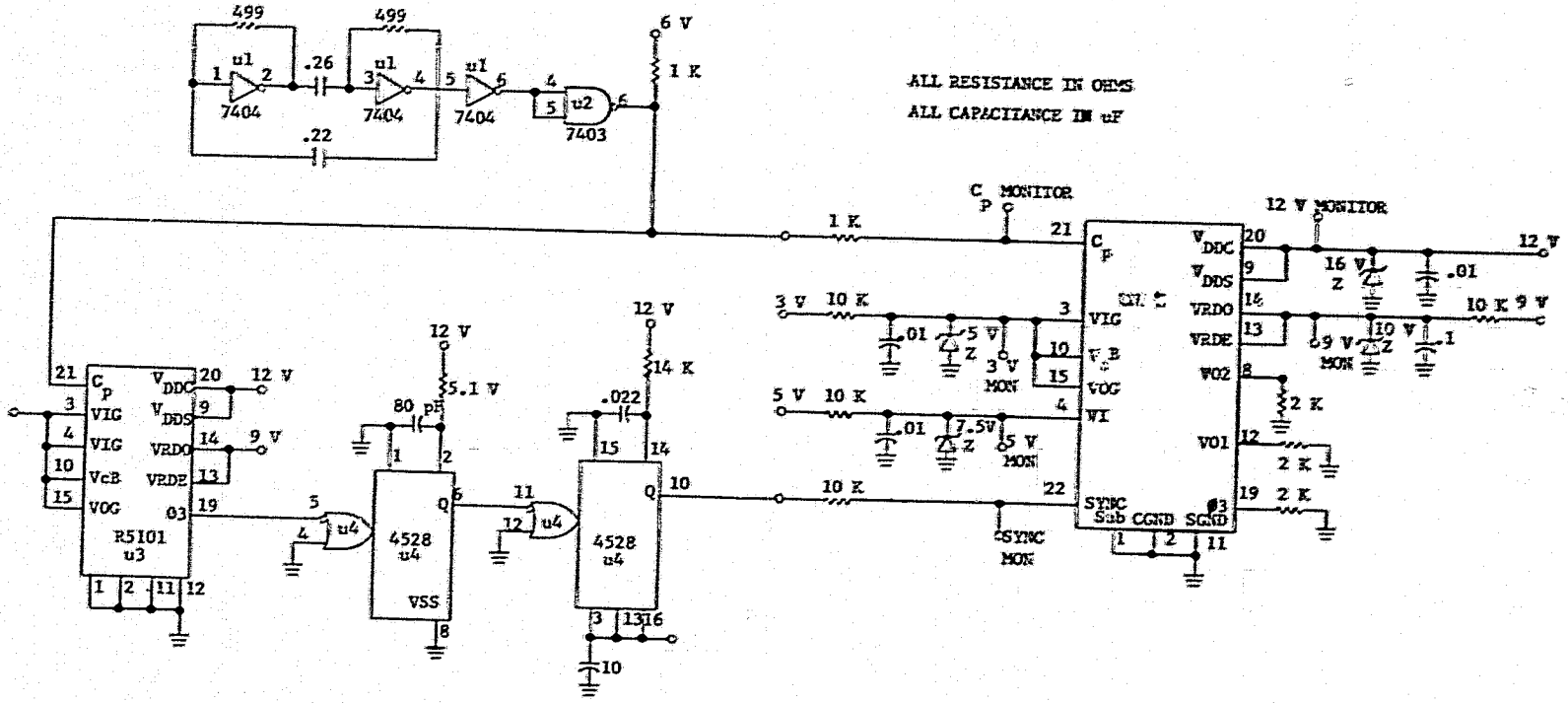


Figure IV-58 Burn In Circuit, R5101

limiting resistor and a Zener diode are in this line. The sync input requires the majority of the control circuitry to drive this device. The clock frequency drives an R5101 which supplies the $\phi 3$ output signal to generate the timing through two miltivibrator circuits to produce the sync input signal. This signal forces all of the R5101 circuits under test to operate with the same phasing. If the sync input occurs at the wrong time or for the wrong length of time, current spikes within the clock circuit on the CCD can result. The construction analysis section discusses the operation of this input. Since there are numerous other gates which are stressed by a dynamic test this input could be held at ground with very little reliability information being lost. This would significantly simplify the burn-in circuit. The 12 volt line going to V_{DDC} and V_{DDS} has a Zener diode and a monitor point. There is not a current limiting resistor in this circuit, however, the power supply was set in current limiting when the devices reached the operating temperature. This is an effective way to limit the current flow for this input. The reset drains were connected to the nominal 9 volts through a 10 kohm limiting resistor and with Zener diode overvoltage protection. The three output circuits were each connected to a 2 kohm load to ground with these resistors being at each socket on the burn-in board. These resistors were high temperature wire wound resistors which could operate at up to 1 watt at 200°C.

The substrate, clock ground, and signal ground were connected together and tied to a common ground.

The 5 KHz operating frequency was chosen so that the parts would be stressed dynamically, however, stray effects related to high frequency operation were avoided.

The two groups of 20 parts each were placed in these burn-in circuits and individually measured to verify proper operation. The burn-in circuits were then placed in the ovens and the 4000 hour life test initiated. S/N 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 41 were operated at 185°C. S/N 24, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 47, 48, 49, 50, and 42 were operated at 170°C. S/N 41 and 42 were two of the devices which had been subjected to the thermal step stress test. They were utilized to obtain 20 devices in each temperature group. Electrical measurements were made at 4, 8, 16, 32, 64, 128, 256, 500, 1000, 2000, and 4000 hours cumulative. The output of each circuit and the monitor points were checked daily. The current level on each power supply was read and recorded at the beginning and end of each period of test. The 12 volt supplies drew about 195 mA for the 170°C test and 150 mA for the 185°C test.

Only one device, S/N 10, from the 185°C temperature group was removed from test during the entire 4000 hours. This part had 48 microamps of leakage current on pin 15 after 1000 hours of test and will be discussed in the failure analysis section. The data obtained will be compiled and discussed in the section on data analysis. There was little significant shift in the device performance during the course of the test.

G. Temperature Cycle

At the completion of the 4000 hour life test 6 devices were subjected to 1000 temperature cycles. Two devices were taken from each of the life test groups and two were removed from test following the environmental screen. The temperature cycle test was performed in accordance with MIL-STD-883, Method 1010, Condition C (150°C to -65°C).

Electrical measurements were taken before temperature cycling and after 20, 50, 250, 500, and 1000 cycles.

Table IV-11 provides the electrical data on these 6 devices at initial test and following 1000 cycles. There appears to be a slight decrease in the gain from these data, however, analysis of the data during the test indicates that the gain fluctuates due to changes in the room temperature at test and also to slight changes in the power supply settings. Control samples were not measured during this testing.

H. Overvoltage Test

Six units were subjected to overvoltage conditions on various pin combinations to determine whether there were any combinations which resulted in permanent damage to the devices. The pins selected included input gates to substrate and overlapping polysilicon layers. The following pin combinations were stressed on each of the six devices: 3 to 1, 3 to 11, 4 to 1, 4 to 11, 10 to 1, 10 to 11, 15 to 1, 15 to 11, 21 to 2, 21 to 11, 22 to 2, 19 to 11, 13 to 8, 8 to 13, 14 to 12, 12 to 14, 9 to 8, and 8 to 9. The first number is positive with respect to the second. For all of these combinations breakdown occurred between 25 and 45 volts and could be repeated numerous times with no change in the level. The parts continued to work properly following this test.

They were then subjected to output short circuit conditions to determine if the analog output or the Ø3 output could be damaged. The short circuit current on the analog outputs was approximately 7.4 mA. The current on the Ø3 output ranged from 84 to 107 mA. With a short circuit condition on these outputs for up to 10 minutes each, no damage occurred.

I. Data Analysis

This section will include a discussion of the deltas which occurred during the course of this testing, and statistics on each of the parameters measured. Life regression curves were not generated due to the small number of failures which occurred.

Electrical measurements were run at -25°C, +25°C, and +55°C during the initial characterization and following the environmental screen tests. Test Control Numbers (TCN) were utilized to keep track of the time of test. The TCNs of interest are shown in Table IV-12.

Table IV-11 Temperature Cycle Electricals, R5101

Drain Current (nA)	Clock Current (mA)	Signal Current (mA)	Offset Voltage (V)	Gain (V/V) Side 1	Gain (V/V) Side 2		Serial Number	Time of measurement	
85	12.84	1.65	3.90	.76	.78		17	initial	
84	12.83	1.64	3.90	.75	.77		17	final	
65	13.42	1.81	4.09	.81	.83		18	initial	
76	13.46	1.74	4.08	.80	.82		18	final	
57	14.03	1.98	4.38	.76	.80		45	initial	
64	13.84	1.92	4.36	.74	.78		45	final	
59	13.37	1.83	4.09	.78	.82		46	initial	
63	13.36	1.79	4.07	.77	.80		46	final	
62	13.69	1.83	4.11	.81	.85		47	initial	
65	13.68	1.80	4.10	.80	.83		47	final	
66	12.73	1.76	3.99	.78	.82		49	initial	
67	12.72	1.74	3.98	.77	.80		49	final	

TABLE IV-12 TCN LIST, R5101

TCN	SEQUENCE	TEST TEMPERATURE
0	INITIAL	25°C
1	INITIAL	-25°C
2	INITIAL	55°C
4	POST ENVIRON	25°C
5	POST ENVIRON	-25°C
6	POST ENVIRON	55°C
117	POST LIFE TEST 185°C	25°C
217	POST LIFE TEST 170°C	25°C

Table IV-13 lists the deltas between the initial measurements and the post environmental screen measurements at +25°C. Table IV-13a shows the control part deltas, and the deltas for the devices which will go into the 185°C life test group. Table IV-13b shows the control part deltas and the deltas for the devices which will go into the 170°C life test group.

The average and standard deviation are given at the bottom. On Table IV-13a S/N 3 was not utilized for taking this average. This part was run three times for TCNO with none of the measurements repeatable. There was evidently a poor connection as this part was very stable during the remainder of the testing.

The control average was subtracted from the average value of the test parts and this value listed along with the percentage change. The only large percentage change is for the noise measurement on side 1. As discussed earlier this parameter was very sensitive to system noise and device warm-up. This change is not considered to be a change in the part's electrical characteristics.The percentage change is not listed for the transfer efficiency due to the very small number involved. A change of 4×10^{-6} for this reading indicates a change of about 10 mV on the voltage read to calculate transfer efficiency. This equation was discussed in the electrical section. As an example, to get the change of 4×10^{-6}, V3 could go from 1.80 volts to 1.81 volts with V2 = 3.3 volts and V1 = 1.7 volts.

This is too small of a change from which to draw any conclusions.

Table IV-13b provides the deltas for the control parts and the parts to go into the 170°C life test. The magnitude of the changes is similar to that of Table IV-13a.

Table IV-14 lists the deltas between the initial measurements and the post environmental screen measurements at -25°C. Control parts are not listed because they were not recorded by the test engineer at the same time as the remainder of the parts. They do not reflect the same test conditions and are therefore invalid for comparison. The comparison does not appear necessary since the largest average delta is only 1.1 percent.

S/N 50 appears to have shifted or one of the two sets of readings was in error. The I_{DDC} reading shifted by -4.5% and the gain on side 1 shifted by -3.5%. The readings on this part during the life test will be examined to determine if the part is changing with operating stress.

Table IV-15 lists the deltas between the initial measurements and the post environmental screen measurements at +55°C. The control parts are not listed for this group for the same reason as the -25°C measurement. They were not recorded at the same time as the remainder of the parts.

TABLE IV-13a MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ 25°C; R5101.

IRD nA	IDDC mA	IDDS mA	VOFFSET (V)	GAIN $X10^{-4}$ SIDE 1	GAIN $X10^{-4}$ SIDE 2	NOISE $X10^{-2}$ (MV) SIDE 1	NOISE $X10^{-2}$ (MV) SIDE 2	CTE $X10^{-6}$ SIDE 1	CTE $X10^{-6}$ SIDE 2	FOR 185°C LIFE TEST SERIAL NUMBER
2	.08	.03	.02	62	100	4	5	-2	1	1-CONTROL
3	.05	.05	.02	53	84	8	9	1	-3	2-CONTROL
2.50	.065	.04	.02	57	92	6	7	-.5	-1	AVERAGE DELTA
-14.4	-.04	-.03	.02	271	313	13	6	-9	-11	3 *TCNO NOT CORRECT
0	.07	.06	.01	70	110	-11	-5	4	2	4
3.4	.05	.06	0	41	57	-8	-16	7	6	6
.3	-.17	.04	-.01	23	19	-21	-15	2	0	7
7	.01	.04	.01	38	73	-14	32	0	-2	8
-2	-.01	.05	0	54	62	-15	-6	3	1	9
1	.03	.02	0	43	64	-10	9	4	3	11
6.9	-.05	.06	-.01	21	21	-1	24	3	2	12
5	.21	.04	.01	36	52	-18	-7	-4	-6	13
0	.08	.02	.01	35	77	-13	26	3	1	14
1.3	.07	.07	.01	61	105	-11	39	4	3	15
-.3	-.10	.03	-.01	27	28	0	-3	4	4	16
2.1	.03	.03	0	30	43	-9	1	3	2	17
1.1	-.03	.05	0	30	57	-18	6	4	3	18
4.1	.03	.01	-.01	8	28	-6	-4	6	5	19
5.8	-.01	.02	-.01	-21	-13	-1	-11	8	8	20
-3	-.01	.03	0	49	73	-6	43	5	4	21
-2	-.55	0	-.03	-31	-54	-9	-12	2	1	22
.5	.02	.01	.01	54	87	-9	5	4	3	41
0.96	-.02	.04	0	32	49	-10	6	3.4	2.2	AVERAGE DELTA
3.37	.15	.02	.01	26	40	6	19	2.6	3.1	STD. DEVIATION
-1.54	-.09	0	-.02	-25	-43	-16	-1	3.9	3.2	(-CONTROL AVERAGE
-2	-0.7	0 0	-0.5	-0.3	-0.5	-32	-2	--	--	PERCENT CHANGE
80	13	1.8	4.1	8500	8500	50	50	999 .610	999 610	TYPICAL VALUE

TABLE IV-13b MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ 25°C; R5101.

I_{RD} (nA)	I_{DDC} (mA)	I_{DDS} (mA)	V_{Offset} (V)	Gain $\times 10^{-4}$ Side 1	Gain $\times 10^{-4}$ Side 2	Noise $\times 10^{-2}$ (mV) Side 1	Noise $\times 10^{-2}$ (mV) Side 2	CTE $\times 10^{-6}$ Side 1	CTE $\times 10^{-6}$ Side 2	FOR 170°C LIFE TEST Serial Number
2	.08	.03	.02	62	100	4	5	-2	1	1 - Control
3	.05	.05	.02	53	84	8	9	1	-3	2 - Control
2.5	.065	.04	.02	57	92	6	7	-.5	-1	Average
4.4	.02	.05	.01	.10	35	-11	-1	7	7	24
6.3	-.07	.06	-.01	0	11	4	-12	4	2	26
1.2	-.13	.04	.01	48	-19	7	53	3	1	27
1.9	-.02	.02	-.01	-24	-30	-9	15	8	7	28
3.5	-.1	.05	-.01	24	7	-31	70	3	2	29
-1	.07	.04	.03	111	144	-2	-7	6	7	30
3.2	.39	.04	.04	145	174	17	-2	11	12	32
3.9	.05	.02	0	171	21	0	3	1	0	33
3.2	-.04	.06	0	65	83	-5	-1	5	3	34
-2	0	.05	-.02	109	155	-7	1	2	-3	35
-2.8	.01	.04	-.02	87	99	-15	-31	3	4	36
3.2	.31	.02	.02	78	86	9	-38	-4	-10	37
4.9	.17	.06	.01	81	97	-2	-14	-2	-3	38
-1	.43	.02	.02	79	138	-2	-1	-4	-8	39
-3.4	.04	.04	.01	14	39	-15	-9	8	8	40
2	.09	.02	.02	57	89	-9	-2	16	18	47
1.9	.02	.09	.01	-24	-64	-14	-64	11	16	48
6.9	.03	.06	.01	13	-2	-7	-1	14	16	49
2.9	-.06	.03	.03	132	96	-15	22	0	3	50
8.1	.16	.02	.01	65	73	-4	-9	-3	-5	42
2.4	.07	.04	.01	62	62	-5.5	-1.4	4.5	3.9	Average Δ
3.1	.15	.02	.02	55	66	10.5	28.5	5.7	7.8	Standard Deviation
-0.1	.005	0	-.01	5	-30	-11.5	-8.4	5	4.9	Average - Control
-0.1	<0.1	0	-0.2	<0.1	-0.4	-23	-17	-	-	Percent Change
80	13	1.8	4.1	8500	8500	50	50	999610	999-610	Typical Value

TABLE IV-14a MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ -25°C

IRD (nA)	IDDC (mA)	IDDS (mA)	V-offset (V)	Gain x10-4 Side1	Gain x10-4 Side2		R5101, FOR 185°C LIFE TEST Serial Number
-1.3	-0.2	0	0	6	20		3
-.7	-.06	0	-.01	-22	-24		4
-1.5	-.02	0	0	-6	-11		6
-.2	.05	-.01	0	-17	-13		7
.6	-.20	-.01	-.01	-23	-27		8
-1.0	-.15	-.01	-.01	-19	-27		9
-2.1	-.06	-0.1	0	-5	-11		11
-.6	-.13	0	0	-14	-15		12
0	-.15	-.01	-.01	-27	-32		13
.7	-.20	-.01	-.01	-14	-16		14
-.5	-.12	-.01	-.01	8	7		15
-2.1	-.09	0	0	4	7		16
-.4	-.01	0	0	2	9		17
-1.0	-.10	0	-.01	3	11		18
-1.1	.03	.01	.01	17	26		19
-.9	.01	0	0	-83	-83		20
-.5	-.15	-.01	-.01	-13	-16		21
-1.0	-.38	0	-.01	-31	-38		22
-.4	-.20	-.01	-.01	3	4		41
-.7	-.10	<.01	<.01	-12	-12		Average
.75	.10	<.01	<.01	22	25		Standard Deviation
-0.9	-0.8	0	0	-0.1	-0.1		Percent Change
80	13	1.8	4.1	8500	8500		Typical Value

TABLE -14b MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ -25°C

IRD (nA)	IDDC (mA)	IDDS (mA)	V- offset (V)	Gain x-10^{-4} Side1	Gain x10^{-4} Side2		R5101 FOR 170°C LIFE TEST Serial Number
-1.8	-.20	-.01	-.01	-80	-113		24
-1.4	-.15	-.01	-.02	-39	-38		26
.5	-.13	0	-.01	-3	6		27
-.1	.01	.01	0	-82	-82		28
-.1	.03	0	0	13	25		29
.9	-.13	-.01	0	-9	2		30
.1	-.21	0	0	-12	-9		32
0	-.03	0	-.01	-18	-5		33
-1.3	-.21	0	.02	27	32		34
-.3	.13	0	.01	3	15		35
.1	-.15	-.01	-.03	2	17		36
-.4	-.13	-.02	0	-1	0		37
-1.7	-.28	-.01	-.01	-16	-18		38
-.9	-.32	0	-.01	-25	-24		39
-1.0	-.12	0	-.01	-50	-55		40
-1.0	-.20	0	-.01	-12	-32		47
-2.5	-.12	.01	0	-55	-56		48
-1.1	-.02	0	.01	32	18		49
13	-.59	-.06	.01	298	129		50
-2.0	-.26	0	-.01	-12	-15		42
-.05	-.15	-.01	<.01	-1.9	-10.1		Average
3.2	.15	.01	.01	77	49		Standard Deviation
0	-1.1	-0.1	0	0	-0.1		Percent Change
80	13	1.8	4.1	8500	8500		Typical Value

TABLE IV-15a MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ 55°C

IRD (nA)	IDDC (mA)	IDDS (mA)	V-offset (V)	Gain x10^{-4} Side1	Gain x10^{-4} Side2		R5101 FOR 185°C LIFE TEST Serial Number
39.8	.57	-.02	-.06	-127	-163		3
19.6	.50	0	0	-53	-63		4
10.6	.56	0	-.01	-56	-49		6
21.4	.36	.01	0	-49	-68		7
19.8	.62	0	-.01	-51	-49		8
15.2	.61	.01	.01	-37	-29		9
9.5	.54	.01	-.01	-69	-66		11
14.9	.74	.01	0	+95	+152		12
26.8	.38	0	-.01	-35	-81		13
23.3	.62	0	0	-26	-53		14
17.1	.58	.01	0	-55	-68		15
7.7	.53	.01	0	-118	-48		16
21.9	.51	0	-.01	-25	-65		17
14.9	.71	.01	.02	-29	-56		18
20.9	.46	0	0	-24	-51		19
-.2	.60	.02	0	-38	-59		20
13.7	.60	.01	0	-40	-58		21
29.2	.96	.02	.11	+800	-195		22
17.4	.47	0	-.01	-51	-39		41
18.1	.57	.005	.001	.6	-58		Average
8.7	.13	.01	.03	198	65		Standard Deviation
23	4.4	0.3	0	0	-0.7		Percent Change
80	13	1.8	4.1	8500	8500		Typical Value

TABLE IV-15b MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ 55°C

IRD (nA)	IDDC (mA)	IDDS (mA)	V- offset (V)	Gain $\times 10^{-4}$ Side1	Gain $\times 10^{-4}$ Side2		R5101 FOR 170°C TEST Serial Number
11.9	.74	.03	.04	-103	76		24
6.6	.68	.01	0	-20	-141		26
16.1	.73	.01	0	+162	-24		27
2.5	.64	.02	.02	-34	-31		28
10.0	.81	.02	.01	99	199		29
21.2	.60	0	.01	-56	-67		30
15.5	.77	.02	0	5	161		32
23.3	.49	0	-.01	-34	-40		33
15.5	.44	0	0	-11	-3		34
22.0	.53	0	0	-11	-25		35
13.4	.51	-.01	-.02	23	3		36
27.8	-.45	0	0	-56	-60		37
22.2	.13	.01		98	61		38
23.2	.53	.01	.01	-17	-18		39
5.8	.54	.01	0	-24	-14		40
5.4	.54	.03	.03	27	87		47
-25.7	.48	.04	.02	19	58		48
8.1	.45	.02	.01	10	35		49
9.3	.44	0	.02	-21	-42		50
23.2	.37	.01	0	-8	-25		42
12.9	.50	.01	.007	2.4	9.5		Average
11.7	.27	.01	.014	60	79		Standard Deviation
16.1	3.8	0.6	0.2	0	0.1		Percent Change
80	13	1.8	4.1	8500	8500		Typical Value

There is more variation in these electrical readings. The fairly consistent change in I_{RD}, I_{DDC}, and gain indicates that a slightly different temperature was used for this measurement. I_{RD} and I_{DDC} increase with temperature and gain decreases with temperature. Calculations on several typical parts indicate a difference in the measurements equal to 4°C. The second reading, TCN6, was taken at 4°C higher than the first reading, TCN2.

Serial numbers 12, 22, 27, 29, and 32 have fairly large gain shifts in the opposite direction. The percentage change are listed in Table IV-16. These are positive changes while the normal change was about -0.5%. The changes in these readings is apparently due to a device shift. The readings on these parts will be examined during the life test for shifts with operating stress.

No conclusive shifts were evident during the environmental testing. The life test offers a better data base to determine any parametric shifts.

Table IV-17 provides the delta shifts for the measurements prior to the 4000 hour life test and following the life test. The percent change has been calculated, however, with the large standard deviation this is not very meaningful. The maximum and minimum changes from Table IV-17 are given in Table IV-18. The deltas for the 185°C group are generally larger than those for the 170°C group. The I_{RD} changes and the noise changes are the largest on this table. They are also the least significant as described in the electrical section. The I_{RD} reading is the charging current for the output transistor gate and was used to check for input gate leakage. Microamp level changes would have indicated a gate breakdown condition. The changes seen in the low nanoamp level are not considered failures. The noise measurements both increased and decreased following the life test. This measurement did not find a general trend for an increase in noise with operating life.

There was in general an increase in I_{DDC}, gain, and transfer efficiency with time. This may be due to a slight shift in the operating point along the transfer function.

The outliers from Table IV-17 are serial numbers, 6, 11, 13, 16, 20, 22, 29, 33, 40, 47, 48, 49 and 50.

The outliers seen prior to the life test were serial numbers 12, 22, 27, 29, 32 and 50.

The data sheets for the parts that are in both of these groups are shown in Table IV-19. These are S/N 22, 29 and 50. Also shown is a control part, S/N 1.

The delta shifts on the control part are given in Table IV-19a for the enitre life test.

TABLE IV-16 PERCENT CHANGE (GAIN), R5101

SERIAL NUMBER	PERCENT CHANGE	
	SIDE 1	SIDE 2
'12	1.1	1.8
22	9.4	2.3
27	1.9	0.3
29	1.2	2.3
32	.1	1.9

TABLE IV-17a MEASUREMENT DELTAS, PRE & POST 4000 HR LIFE TEST, @ 25°C; R5101

IRD	IDDG	IDDC	V-offset	Gain x10^{-4}		Gain x10^{-4}		Noise x10^{-2}		CTE x10^{-6}		185°C
(nA)	(mA)	(mA)	(V)	Side1	Side2	Side1	Side2	Side1	Side2	Side1	Side2	Serial Number
.9	-.03	-.01	-.01	-42	-36	7	-10	2	2			1 - Control
.9	-.02	-.05	0	-22	-24	-7	-16	3	2			2 - Control
.9	-.025	-.03	-.005	-32	-30	0	-13	2.5	2			Average
9.3	.01	.05	0	-65	-46	-18	8	2	0			3
-6.0	.03	.03	.01	2	-47	-4	1	25	24			4
16.4	.06	.07	.01	-342	-348	4	2	65	60			6
-2.9	.51	.02	.03	110	-19	34	23	21	23			7
-1.7	.03	.01	.01	74	52	-15	-4	13	13			8
1.3	.24	0	.02	33	5	6	1	1	2			9
-20.8	-.01	.08	0	-311	-253	-8	6	67	62			11
-5.9	.39	.03	.02	121	59	-1	-2	27	24			12
75.8	.65	.01	.03	128	52	40	22	4	5			13
0	.11	0	.02	69	45	10	7	1	1			14
0	.06	-.01	.01	44	19	22	4	1	2			15
-9.4	.19	.03	0	-117	-109	1	-5	25	22			16
2.2	.09	-.01	.01	7	3	-8	-2	-7	-8			17
-5.3	.08	.02	0	117	74	3	7	19	19			18
-4.9	.06	.02	.01	49	22	-1	5	13	13			19
20.2	.10	-.07	.02	372	338	-2	-4	-71	-67			20
15.0	.12	-.01	.02	35	26	-10	12	-12	-10			21
1.7	1.03	.01	.05	124	69	0	8	10	12			22
4.4	.02	-.02	.01	-35	-57	0	4	-11	-12			41
3.0	0.20	.01	.015	22	-6	2.8	4.9	11	10			Average
20.1	0.27	.03	.013	158	138	15	7.8	29	27			Standard Deviation
2.1	.23	.04	.02	54	24	2.8	17.9	8.5	8			Average-Control
2.6	1.8	2.2	0.5	0.6	0.3	5.6	36	-	-			Percent Change
80	13	1.8	4.1	8500	8500	50	50	999610	999610			Typical Value

TABLE IV-17b MEASUREMENT DELTAS, PRE & POST 4000 HR LIFE TEST, @25°C; R5101

IRD (nA)	IDDC (mA)	IDDS (mA)	V-offset (V)	Gain x10^{-4} Side1	Gain x10^{-4} Side2	Noise x10^{-2} (mV) Side1	Noise x10^{-2} (mV) Side2	CTE x10^{-6} Side1	CTE x10^{-6} Side2	170°C Serial Number
.9	-.03	-0.1	-0.1	-42	-36	7	-10	2	2	1 - Control
.9	-.02	-.05	0	-22	-24	-7	-16	3	2	2 - Control
.9	-.025	-.03	-.005	-32	-30	0	-13	2.5	2	Average
-5.3	0	.02	.01	-65	-54	-2	7	28	28	24
-.9	.13	.01	.02	93	49	47	3	0	0	26
-5.1	.25	.02	.01	118	69	-51	-18	18	16	27
-4.2	.14	.03	.03	34	4	8	6	22	21	28
-6.6	.47	.04	.04	182	106	9	4	27	26	29
-4.0	.04	.01	-.01	59	21	20	-5	6	-91	30
-9.0	.01	.02	-.02	46	-18	44	-27	24	23	32
1.4	.10	.01	.02	194	127	-3	6	10	12	33
-8.1	.08	.03	.02	47	26	19	10	25	21	34
-3.7	.07	0	-.01	59	54	-11	-3	15	12	35
-1.3	.14	.01	.03	79	29	30	7	4	3	36
3.8	.26	0	.02	41	5	0	-6	7	8	37
4.1	.41	0	.02	65	8	81	49	8	9	38
-1.0	.18	0	.02	53	25	11	5	14	15	39
-10.6	.06	.05	.02	169	181	39	1	60	59	40
-10.5	-.10	.03	-.02	143	124	0	6	23	22	47
12.9	.06	-.03	-.03	326	266	90	29	28	22	48
-1.9	.08	.01	.01	162	103	-1	9	-7	-5	49
-16.9	1.41	.06	-.01	291	38	-34	-2	38	54	50
.1	.76	.01	.03	42	126	0	7	11	9	42
-3.3	.23	.017	.01	107	64	15	4.4	18	13	Average Delta
6.4	.34	.020	.02	93	75	34	15	15	29	Standard Deviation
-4.2	.25	.05	.01	139	94	15	17.4	15.5	11	Average - Control
-5.2	1.9	2.8	0.2	1.6	1.1	30	35	-	-	Percent Change
80	13	1.8	4.1	8500	8500	50	50	999610	999610	Typical Value

TABLE IV-18a MAXIMUN SHIFTS, 185°C GROUP, R5101

IRD (nA)	IDDC (mA)	IDDS (mA)	V-offset (V)	Gain x10^{-4} Side1	Gain x10^{-4} Side2	Noise x10^{-2} Side1	Noise x10^{-2} Side2	CTE x10^{-6} Side1	CTE x10^{-6} Side2	
75.8	1.03	.08	.05	372	338	40	23	67	62	Maximum Positive
95	7.9	4.4	1.2	4.4	4.0	80	46	-	-	Percent Change
-20.8	-0.01	-0.07	0	-342	-348	-18	-5	-71	-67	Maximum Negative
-26	0	-3.9	0	-4.0	-4.1	-36	-10	-	-	Percent Change
80	13	1.8	4.1	.85	.85	.50	.50	.999610	.999610	Typical Value

TABLE IV-18b MAXIMUN SHIFTS, 170°C GROUP, R5101

IRD (nA)	IDDC (mA)	IDDS (mA)	V OFF-SET (V)	GAIN X10^{-4} SIDE1	GAIN X10^{-4} SIDE2	NOISE X10^{-2} SIDE1	NOISE X10^{-2} SIDE2	CTE X10^{-6} SIDE1	CTE X10^{-6} SIDE2	
12.9	1.41	.06	.04	326	266	90	49	38	54	MAXIMUN POSITIVE
16	11	3	1	3.8	3.1	180	98	-	-	PERCENT CHANGE
-16.9	-.10	-.03	-.03	-65	-54	-51	-27	-7	-91	MAXIMUN NEGATIVE
21	.08	1.7	0.7	0.7	.06	100	54	-	-	PERCENT CHANGE
80	13	1.8	4.1	.85	.85	.50	.50	.999610	.999610	TYPICAL VALUE

TABLE IV-19a OUTLIER MEASUREMENT DELTAS, R5101 S/N 1(CONTROL)

TEST	IADC mA	IDDC mA	IDDS mA	VOFFSET V	GAIN 2	GAIN 1	NOISE 2 mV	NOISE 1 mV	CTE 2	CTE 1
4	75.00	13.34	1.74	4.08	0.8540	0.8280	0.69	0.60	0.999609	0.999615
107	77.00	13.30	1.74	4.07	0.8443	0.8229				
108	75.30	13.25	1.76	4.08	0.8509	0.8268				
109	76.90	13.31	1.75	4.08	0.8531	0.8274				
110	77.50	13.32	1.74	4.07	0.8482	0.8220				
111	77.00	13.40	1.75	4.08	0.8535	0.8278				
112	76.90	13.37	1.75	4.08	0.8535	0.8270				
113	77.10	13.31	1.74	4.07	0.8475	0.8237				
114	76.00	13.30	1.73	4.08	0.8458	0.8216				
115	75.50	13.28	1.74	4.08	0.8500	0.8255				
116	76.40	13.27	1.74	4.06	0.8463	0.8213				
117	75.90	13.31	1.74	4.07	0.8498	0.8244	0.76	0.50	0.999608	0.999618
MEAN	76.40	13.30	1.74	4.07	0.8497	0.8248	0.72	0.55	0.999607	0.999617
S.D.	0.82	0.02	0.01	0.01	0.0032	0.0024	0.04	0.05	0.000001	0.000001
		DELTA SHIFTS								
107	2.00	-0.05	0.00	-0.01	-0.0097	-0.0052				
108	0.30	-0.10	0.01	0.00	-0.0031	-0.0012				
109	1.90	-0.04	0.01	-0.00	-0.0009	-0.0006				
110	2.80	-0.03	0.00	-0.00	-0.0058	-0.0061				
111	2.50	-0.05	0.00	-0.00	-0.0004	-0.0002				
112	1.90	-0.07	0.01	-0.00	-0.0005	-0.0010				
113	2.10	-0.03	0.00	-0.01	-0.0055	-0.0043				
114	1.00	-0.04	-0.01	-0.02	-0.0082	-0.0064				
115	0.50	-0.07	-0.00	0.00	-0.0040	-0.0026				
116	1.40	-0.07	-0.02	-0.02	-0.0077	-0.0067				
117	0.90	-0.03	-0.01	-0.01	-0.0042	-0.0036	0.07	-0.10	0.000002	0.000002

S/N 22 is given in Table IV-19b. The clock current on this device is the highest on any of the 50 devices tested. This was about 36 mA. The change of 1.03 mA is a 2.9% shift. This device does have a short between transfer electrodes and this will contribute to the instabilities. The cause for the high current will be discussed in the failure analysis section.

S/N 29 is given in Table IV-19c. The instability of the gain is envident. This is not a continual degradation but rather fluctuates with time.

S/N 50, Table IV-19d, also exhibits instability with operating life.

The transfer efficiency does not show degradation with time as postulated. There is a slight increase on most parts. The largest change seen was a -91×10^{-6} on serial number 30. This was a change from .999660 to .999569. This represents a change of about 0.3 volts on the V3 reading.

Tables IV-20 and IV-21 contain statistics on each of the parameters measured except for input leakage current. Table IV-20 covers the parameters at +25°C, -25°C, and +55°C at initial characterization. The seven devices which had shift register shorts were not used for the clock current statistics. The largest variation seen within a parameter is the noise measurement. This variation was discussed previously. The gain is also seen to vary about 25% from min to max. This is due to manufacturing differences. Table IV-21 covers the same parameters following the life test. These include the 170°C life test and the 185°C life test. There is very little difference between the pre and post life test statistics.

The conclusion reached from this data analysis is that there is little change with operating life on surface channel CCDs. The larger changes seen are on parts that fluctuate during the testing rather than changes that would indicate a temperature accelerated shift in one direction.

J. Failure Analysis

A summary of all the R5101 failures which occurred during the course of this testing is given in Table IV-22. Failure analysis was performed on these and is discussed below.

Serial numbers 5 and 25 failed due to leakage on pin 22 at initial electrical test.

Serial number 23 was removed from test following the 160 hour, 55°C burn-in. The gain was very erratic at the different measurement points.

Serial number 31 was removed from test following the 160 hour, 55°C burn-in. This device had an increase in clock current of 20 mA.

TABLE IV-19b OUTLIER MEASUREMENT DELTAS, R5101 S/N 22

TEST	IDDE mA	IDDC mA	IDDS mA	VOFFSET V	GAIN 2	GAIN 1	NOISE 2 mV	NOISE 1 mV	CTE 2	CTE 1
4	98.00	36.87	1.55	3.79	0.7116	0.7089	0.47	0.35	0.999641	0.999634
107	100.10	37.05	1.57	3.85	0.7249	0.7217				
108	98.00	36.23	1.57	3.83	0.7201	0.7179				
109	100.00	36.86	1.57	3.84	0.7274	0.7225				
110	100.10	36.47	1.56	3.82	0.7198	0.7137				
111	100.00	36.85	1.56	3.84	0.7207	0.7195				
112	99.30	36.86	1.57	3.84	0.7265	0.7215				
113	99.90	37.03	1.57	3.85	0.7295	0.7244				
114	100.10	36.93	1.55	3.84	0.7145	0.7049				
115	97.70	36.16	1.55	3.81	0.7142	0.7120				
116	98.10	36.84	1.56	3.83	0.7230	0.7139				
117	99.70	36.90	1.55	3.84	0.7249	0.7158	0.47	0.43	0.999651	0.999646
MEAN	99.25	36.85	1.56	3.83	0.7214	0.7169	0.47	0.39	0.999646	0.999640
S.D.	0.95	0.37	0.01	0.02	0.0054	0.0057	0.00	0.04	0.000005	0.000005
		DELTA SHIFTS								
107	2.10	1.18	0.02	0.06	0.0133	0.0128				
108	0.00	0.36	0.02	0.03	0.0085	0.0090				
109	2.00	0.99	0.02	0.05	0.0158	0.0136				
110	2.10	0.60	0.01	0.03	0.0082	0.0048				
111	2.00	0.98	0.01	0.05	0.0091	0.0106				
112	1.30	0.99	0.02	0.05	0.0150	0.0126				
113	1.90	1.16	0.02	0.05	0.0182	0.0155				
114	2.10	1.06	0.01	0.04	0.0031	-0.0040				
115	-0.30	0.29	0.00	0.02	0.0027	0.0031				
116	0.10	0.77	0.01	0.04	0.0116	0.0100				
117	1.70	1.03	0.01	0.05	0.0124	0.0069	-0.00	0.08	0.000010	0.000012

TABLE IV-19c OUTLIER MEASUREMENT DELTAS, R5101 S/N 29

TEM	IADC mA	IDDC mA	IDDS mA	VOFFSET V	GAIN 2	GAIN 1	NOISE 2 mV	NOISE 1 mV	CTE 2	CTE 1
4	73.50	13.31	1.81	4.20	0.8392	0.8034	0.57	0.51	0.999603	0.999623
207	69.90	13.35	1.84	4.23	0.8568	0.8184				
208	67.20	13.31	1.86	4.23	0.8595	0.8213				
209	68.20	13.37	1.86	4.23	0.8633	0.8229				
210	67.90	13.37	1.86	4.23	0.8556	0.8147				
211	65.70	13.31	1.86	4.22	0.8622	0.8217				
212	65.00	13.29	1.87	4.22	0.8576	0.8167				
213	64.00	13.30	1.88	4.23	0.8645	0.8230				
214	64.00	13.41	1.86	4.23	0.8308	0.7977				
215	63.40	13.20	1.86	4.22	0.8471	0.8075				
216	65.70	13.22	1.85	4.22	0.8471	0.8071				
217	66.90	13.48	1.85	4.23	0.8575	0.8140	0.66	0.54	0.999630	0.999649
MEAN	66.78	13.31	1.85	4.22	0.8541	0.8140	0.62	0.53	0.999617	0.999636
S.D.	2.75	0.12	0.02	0.01	0.0085	0.0080	0.05	0.02	0.000013	0.000013
		DELTA SHIFTS								
207	-3.60	0.04	0.03	0.03	0.0175	0.0150				
208	-6.30	0.00	0.05	0.03	0.0203	0.0179				
209	-5.30	0.06	0.05	0.03	0.0241	0.0195				
210	-5.60	0.06	0.05	0.03	0.0164	0.0113				
211	-7.80	0.00	0.05	0.02	0.0230	0.0184				
212	-8.50	0.27	0.05	0.02	0.0184	0.0134				
213	-9.50	0.37	0.06	0.03	0.0253	0.0197				
214	-9.50	0.39	0.05	0.03	-0.0004	-0.0057				
215	-11.10	0.19	0.05	0.02	0.0079	0.0042				
216	-7.80	0.21	0.04	0.02	0.0078	0.0037				
217	-5.50	0.47	0.04	0.04	0.0182	0.0136	0.09	0.04	0.000027	0.000026

TABLE IV-19d OUTLIER MEASUREMENT DELTAS, R5101 S/N 50

TSN	IRDE mA	IDDC mA	IDDS mA	VOFFSET V	GAIN 2	GAIN 1	NOISE 2 mV	NOISE 1 mV	CTE 2	CTE 1
4	62.30	13.39	1.85	4.17	0.8449	0.8172	0.89	0.53	0.999677	0.999685
207	43.90	14.61	1.92	4.18	0.8715	0.8232				
208	49.70	14.37	1.91	4.15	0.8605	0.8115				
209	46.00	14.65	1.93	4.17	0.8771	0.8246				
210	46.00	14.93	1.93	4.17	0.8591	0.8075				
211	43.10	14.68	1.95	4.17	0.8779	0.8243				
212	41.20	14.71	1.95	4.17	0.8727	0.8184				
213	41.90	15.29	1.95	4.18	0.8767	0.8229				
214	42.10	15.45	1.93	4.17	0.8481	0.7947				
215	33.20	14.77	1.95	4.16	0.8597	0.8082				
216	53.60	16.08	1.88	4.15	0.7714	0.8223				
217	46.00	15.40	1.91	4.16	0.8740	0.8210	0.55	0.51	0.999715	0.999739
MEAN	46.56	14.91	1.92	4.17	0.8578	0.8163	0.72	0.52	0.999696	0.999712
S.D.	6.36	0.94	0.03	0.01	0.0282	0.0088	0.17	0.01	0.000019	0.000027
		DELTA SHIFTS								
207	-14.00	0.62	0.07	0.01	0.0256	0.0060				
208	-13.20	0.39	0.05	-0.02	0.0157	-0.0057				
209	-16.90	0.66	0.08	0.00	0.0323	0.0074				
210	-16.90	0.94	0.08	0.00	0.0142	-0.0098				
211	-19.80	0.69	0.10	-0.00	0.0330	0.0071				
212	-21.70	0.72	0.10	0.00	0.0278	0.0012				
213	-21.00	1.31	0.10	0.01	0.0318	0.0057				
214	-20.80	1.46	0.08	-0.00	0.0032	-0.0225				
215	-24.70	0.78	0.10	-0.01	0.0149	-0.0091				
216	-9.30	2.10	0.03	-0.02	-0.0735	0.0051				
217	-16.90	1.41	0.06	-0.01	0.0291	0.0038	-0.34	-0.02	0.000038	0.000054

Table IV-20 Initial Electrical Characterization Parameter Statistics, R5101

Parameter	Test Conditions		Spec. Limits Typical2	Units	Test Data Summary min.	max.	mean	std. dev.
Driver Current	Note 1	-25°C	8	mA	13.31	15.85	14.33	0.50
		+25°C			12.57	14.05	13.12	0.35
		+55°C			14.70	15.79	15.02	0.29
Signal Current	Note 1	-25°C	8	mA	1.62	2.11	1.84	0.13
		+25°C			1.55	1.97	1.71	0.12
		+55°C			1.52	1.89	1.68	0.11
Offset Voltage	Note 1 V_{IN} = 0.0V	-25°C	-	V	4.02	4.58	4.27	0.14
		+25°C			3.82	4.36	4.04	0.15
		+55°C			3.47	4.22	3.90	0.16
Gain Side 1	Note 1 Delta V_{IN} = 1.0 V	-25°C	0.6	V/V	.7513	1.0007	.8628	.1334
		+25°C			.5606	.8320	.7719	.0507
		+55°C			.5836	.8037	.7306	.0440
Gain Side 2	Note 1 Delta V_{IN} = 1.0 V	-25°C	0.6	V/V	.7679	1.0292	.9134	.0581
		+25°C			.6576	.8672	.7950	.0459
		+55°C			.5837	.8179	.7574	.0512
Noise Side 1	Note 1 V_{IN} = 5.0 V	-25°C	-	mV	0.39	0.77	0.53	0.08
		+25°C			0.37	1.72	0.53	0.10
Noise Side 2	Note 1 V_{IN} = 5.0 V	-25°C	-	mV	0.46	1.12	0.64	0.12
		+25°C			0.41	1.27	0.69	0.16
Transfer Eff. Side 1	Note 1	-25°C	-		.999497	.999792	.999645	.000069
		+25°C			.999509	.999785	.999652	.000073
		+55°C			.999515	.999772	.999647	.000059
Transfer Eff. Side 2	Note 1	-25°C	-		.999487	.999782	.999632	.000070
		+25°C			.999543	.999782	.999650	.000067
		+55°C			.999539	.999764	.999654	.000053

Note 1 - V_{DD}=12 V, Ø3 out load = 1.5 kohm, V01 and V02 load = 2 kohm, sampling frequency = 62.5 KHz at -25°C and +25°C, 175 KHz at +55°C.

Note 2 - No maximum and minimum specifications available.

Table IV-21 Parameter Statistics, Post Life Test, R5101

Parameter	Test Conditions	Life Test Temp.	Spec. Limits Typical[2]	Units	Test Data Summary min.	max.	mean	std. dev.
Driver Current	Note 1	170°C	-	mA	12.76	15.40	13.39	0.63
		185°C			12.86	13.76	13.19	0.26
Signal Current	Note 1	170°C	-	mA	1.56	2.01	1.78	0.14
		185°C			1.55	2.02	1.74	0.12
Offset Voltage	Note 1 V_{IN} = 0.0 V	170°C	-	V	3.80	4.32	4.09	0.14
		185°C			3.84	4.32	4.03	0.13
Gain Side 1	Note 1 Delta V_{IN} = 1.0 V	170°C	-	V/V	.6948	.8464	.7927	.0334
		185°C			.6804	.8401	.7682	.0478
Gain Side 2	Note 1 Delta V_{IN} = 1.0 V	170°C	-	V/V	.7163	.8625	.8217	.0382
		185°C			.6962	.8648	.7911	.0524
Noise Side 1	Note 1 V_{IN} = 5.0 V	170°C	-	mV	0.36	0.97	0.52	0.13
		185°C			0.39	0.69	0.50	0.08
Noise Side 2	Note 1 V_{IN} = 5.0 V	170°C	-	mV	0.47	1.45	0.80	0.27
		185°C			0.47	1.20	0.70	0.20
Transfer Eff. Side 1	Note 1	170°C	-		.999522	.999788	.999671	.000076
		185°C			.999552	.999788	.999662	.000067
Transfer Eff. Side 2	Note 1	170°C	-		.999520	.999787	.999668	.000073
		185°C			.999553	.999791	.999661	.000075

Note 1 - V_{DD}=12 V, Ø3 out load = 1.5 kohm, V01 and V02 load = 2 kohm, sampling frequency = 62.5 KHz at -25°C and +25°C, 175 KHz at +55°C.

Note 2 - No specifications available for post life test electricals.

TABLE IV-22 FAILURE SUMMARY, R5101

S/N	FAILURE TIME	FAILURE CLASS	AFFECTED PARAMETER	PHYSICAL CAUSE
7	INITIAL ELECTRICAL CHAR.	PARAMETRIC	CLOCK CURRENT	MANUF DEFECT INCOMPLETE POLYSILICON ETCH
13	"	"	"	"
22	"	"	"	"
37	"	"	"	"
38	"	"	"	"
39	"	"	"	"
42	"	"	"	"
5	INITIAL ELECTRICAL CHAR.	CATASTROPHIC	INPUT LEAKAGE PIN 22	GATE OXIDE SHORT
25	"	"	"	"
23	55°C BURN-IN, POST 160 HR.	PARAMETRIC	GAIN	NONE DETECTED
31	55°C BURN-IN, POST 160 HR.	PARAMETRIC	CLOCK CURRENT	MANUF DEFECT PARTICLE
10	185°C LIFE, POST 1000 HR.	PARAMETRIC	INPUT LEAKAGE PIN 15	INPUT PROTECT DIODE LEAKAGE

Serial number 10 was removed from life test following 1000 hours at 185°C. Leakage current on pin 15 had increased to 48 microamps.

Serial numbers 38, 39, and 42 were analyzed following the life test to determine the cause for the higher clock current levels on 7 of the 50 devices on this study.

The failure analysis reports were written as they were performed and include the history, the cause of the failure, the conclusion, and the test method and disclosure.

The five failure analysis reports follow:

1. R5101, S/N 5

   History: Part failed initial leakage measurement on pin 22. This pin measured 109 microampe, which is the current limitation of the test tool.

   Cause: Cause of the leakage current was a dielectric breakdown which caused a short between the polysilicon gate and the silicon.

   Conclusion: The cause of the dielectric breakdown was most likely an electrostatic discharge during handling. This part was fully functional as received except that it could not be synchronized with other devices since the sync input was shorted to ground. It is likely that this part was damaged prior to receipt at MMC but is was not detected to be a failure since the parametrics on it were acceptable.

   Test Method and Disclosure: Pin to pin electrical measurement found pin 22 (sync input) to be shorted to pin 2 (clock ground). This was a resistive short of 1,000 ohms. The input structure is as shown in Figure IV-59 and in the photograph in Figure IV-60. A portion of the glass passivation was chemically removed using hydrofluoric acid fumes. The part was mechanically probed and the failure reverified. The metallization was mechanically scribed open and the failure was isolated to transistor Q1. This is shown in Figure IV-61. The aluminum metallization was chemically removed over the polysilicon gate and the short was therefore isolated to be between the polysilicon and the silicon. The part was examined in the Scanning Electron Microscope and the failure site was documented (Figures IV-62 and IV-63). This occurs at the oxide step into the thin oxide region for the transistor. This is the typical location and appearance for an electrostatic discharge overstress.

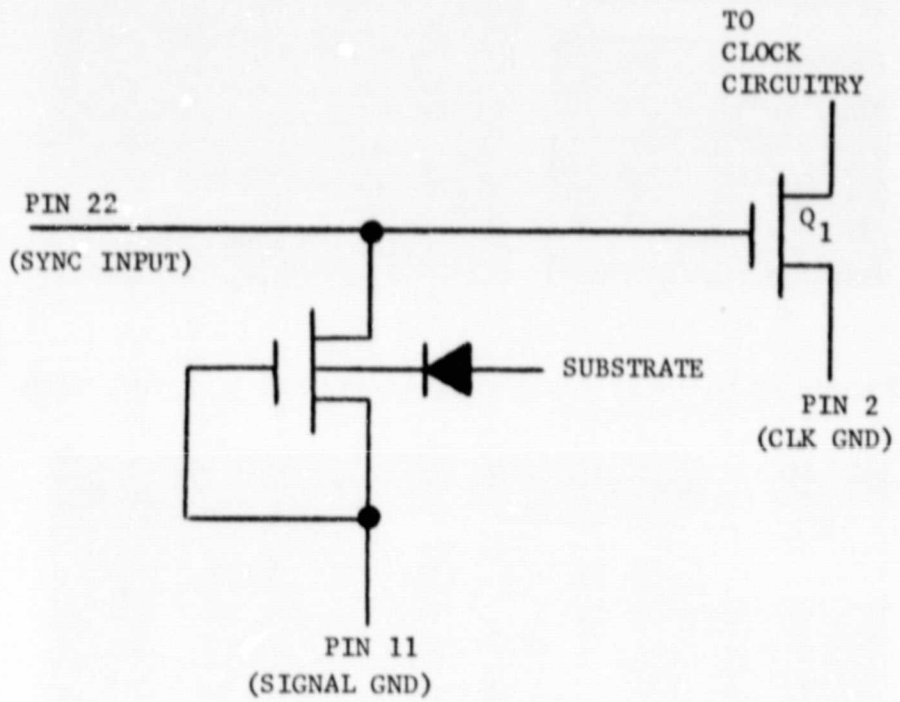


Figure IV-59 Schematic, Sync Input Circuit, R5101

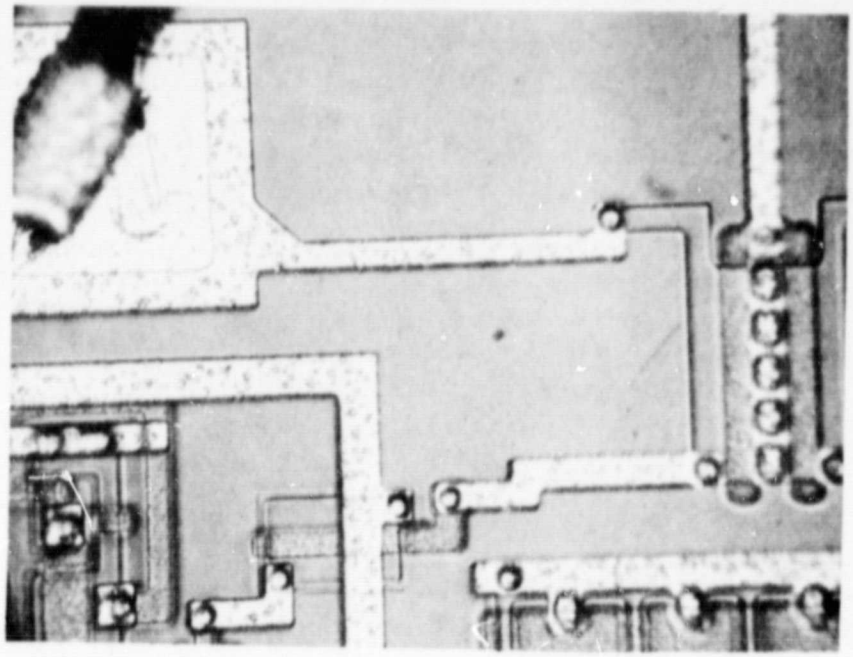


Figure IV-60 Sync Input Photograph, S/N 5, R5101; X400

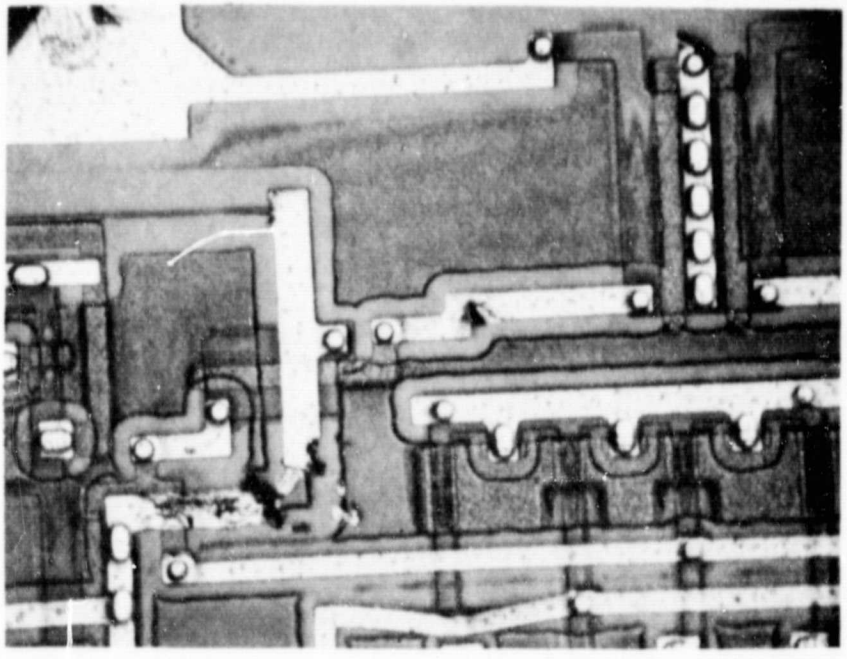


Figure IV-61 Sync Input Photograph, S/N 5, R5101, Failure Isolated; X460

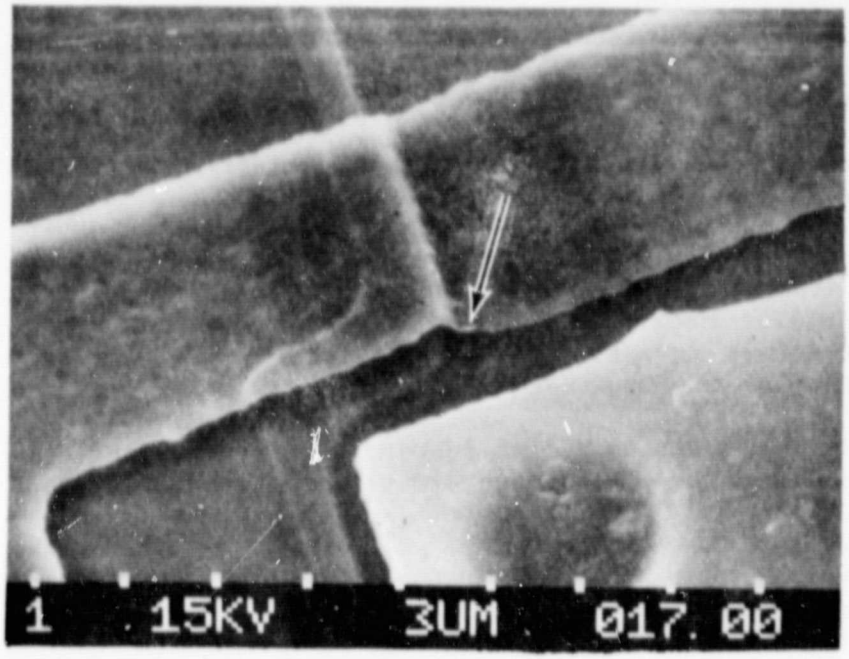


Figure IV-62 SEM Micrograph, Failure Site at Arrow, R5101; X6000

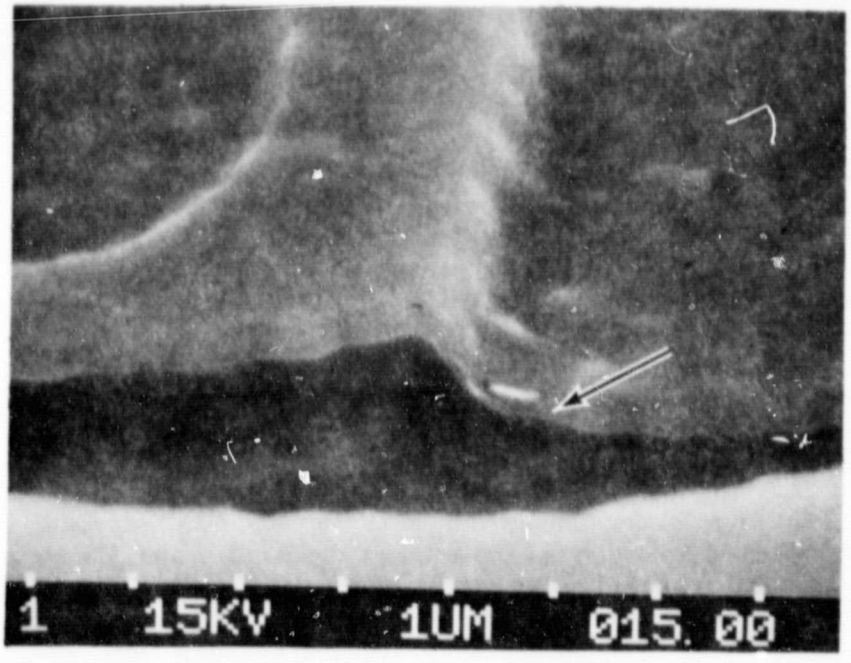


Figure IV-63 SEM Micrograph, Failure Site at Arrow, R5101; X15,000

2. R5101, S/N 25

History: Part failed initial leakage measurement on pin 22. This pin measured 1.5 microamps at the 11 volt measurement point of the leakage test tool.

Cause: Cause of the leakage current was dielectric breakdown which caused a short between the gate and the silicon.

Conclusion: The cause of the dielectric breakdown was most likely an electostatic discharge during handling. This is an identical failure mode to that seen on serial number 5 except that it is not as severe. Again it is likely that this part was damaged prior to receipt at MMC.

Test Method and Disclosure: Pin to pin electrical measurement found pin 22 (sync input) to have 350 nanoamps leakage current at ten volts to pin 2 (clock ground). This part was examined on the light microscope and then a portion of the glass passivation was chemically removed. Due to the low leakage involved an attempt was made to view the failure site utilizing the Electron Beam Induced Current (EBIC) mode on the SEM. No site could be identifed. The input transistor was then mechanically isolated and the gate probed. This transistor was identified as Q1 in the analysis on serial number 5. The 350 nanoamps of leakage current was still present with the transistor completely isolated. SEM examination of the polysilicon gate could not find the location of the failure site.

3. R5101, S/N 23

History: S/N 23 was removed from the test program following the 160 hour, 55 ^{o}C burn-in. The gain on side 1 was very erratic. The following values were measured for this gain: initial = .56, post environmental screen test = .65, post 160 hour burn-in = .58, at time of analysis = .67.

Cause: The cause for the shift in the gain was a shift in the low level output voltage used to calculated the gain. This voltage shifted from 1.87 to 2.01. The upper voltage stayed at about 2.55.

Conclusion: The operating range on this device was narrower than on most of the other circuits. This lead to a nonlinear and very temperature sensitive output voltage level for the low level. This caused the gain to be erratic. The operating range is affected by many manufacturing parameters and the fact that this part is different does not mean that it is a failure but only that there was a variation in its construction.

Test Method and Disclosure: Pin-to-pin electricals found no leakage currents. It was then operated in the test tool and the low level output used in calculating the gain was found to be erratic and very temperature sensitive.

The input voltage was varied and the output level measured. S/N 39 was used as a control. These values are given in Table IV-23.

TABLE IV-23 ELECTRICAL CHARACTERISTICS, R5101

V_{IN}		5.7	5.5	5.2	5.1	5.0	4.9	4.8
V_{OUT}	S/N 23	1.94	1.94	1.94	2.00	2.07	2.14	2.20
	S/N 39	1.42	1.56	1.78	1.86	1.94	2.02	2.09

This shows that the lowest level the output can go to is 1.94 on S/N 23.

The part was opened and examined on the microscope with no apparent problems noted.

4. R5101, S/N 31

History: Serial Number 31 was removed from test following the 160 hour, 55 degree C burn-in. There was an increase in the clock current from 14 mA to 34 mA. The current measured immediately prior to the failure analysis was 29 mA.

Cause: The cause of the increase in the clock current was a layer to layer short between the ∅3 and ∅2 clocks.

Conclusion: There was contamination present on the die surface which occurred during the manufacture of the part following the deposition of the first polysilicon layer and before the second polysilicon layer. Due to the increased surface relief and the location of this particle, the insulating oxide layer did not provide adequate electrical isolation between the two layers. A sight decrease in the transfer efficiency from .99976 to .99969 on side 1 and from .99977 to .99972 on side 2 was caused by this short. This and the increased clock current were the only parameters affected by this short. Additional analysis will be performed on the other 7 devices which exhibited high current during this testing. These parts did not shift during the course of the program but the high current is likely indicative of a similar type of condition.

Test Method and Disclosure: Electrical Measurement using the test tool verified the high clock current. It was determined that this high current could be produced by setting the sync input, the clock input, the substrate and clock ground at

ground and taking V_{DDC} high. This DC configuration would allow the part to be more easily probed to isolate the failure. Utlilizing the schematic developed during the construction analysis several points within the circuit were probed. No abnormal readings were noted. Voltage drop measurements were then taken along the V_{DDC} metallization to follow the current flow into the device. The ∅3 output transistor was found to be drawing the high current. This indicated that there was a short in the shift register section. The voltage levels on the output of ∅3 were then measured. The high level was 3.0 volts and the low level was 0.47 volts. It appeared that the output was supplying current when the output level was high and was sinking current when the output was low. Measurements between ∅3 and the other three clocks found a resistive path of about 200 ohms to ∅2. A control part was opened and probed at this point to verify that this condition should not exist. ∅3 to the other three gates measured open as expected. Voltage drop measurements were then made along the ∅3 metallization to find the point at which the high current flow stopped. This point will be apparent when the voltage drop between two adjacent points goes to zero. This point was isolated to be in the third column of the shift register and the most likely site was photographed and is shown in Figure IV-64. Further probing was performed at this time and the failure site was verified to be between the two probe marks seen in the SEM micrograph in Figure IV-65. The short is between the bottom layer polysilicon which is connected to the center metallization stripe and the overlying polysilicon which is connected to the metallization on the right hand side. This area includes two electrode pairs. Examination of these two electrode pairs found the site shown in Figures IV-66 and IV-67. This contamination occurred during the manufacturing process following the first polysilicon deposition and created a weak point in the oxide isolating the two polysilicon layers.

5. R5101, S/N 10

History: Serial Number 10 was removed from the 185 °C life test group following 1000 hours of test. Pin 15 measured 48 uA at this time. In addition to S/N 10, serial numbers 8, 13, 21, 37, 38, and 48 were analyzed at the end of the life test for leakage conditions.

Cause: The cause of the leakage was junction degradation on the input protect network.

Conclusion: The current leakage developed due to the high temperature reverse bias operation of the input protect transistor. The pins that were found to develop leakage current were those which were physically closest to the output amplifier. This area would be at the highest temperature on the chip due to the power dissipation in the amplifier. The increased die temperature would increase the leakage currents in that area. This increase in leakage would then enhance any current generation sites along the junction.

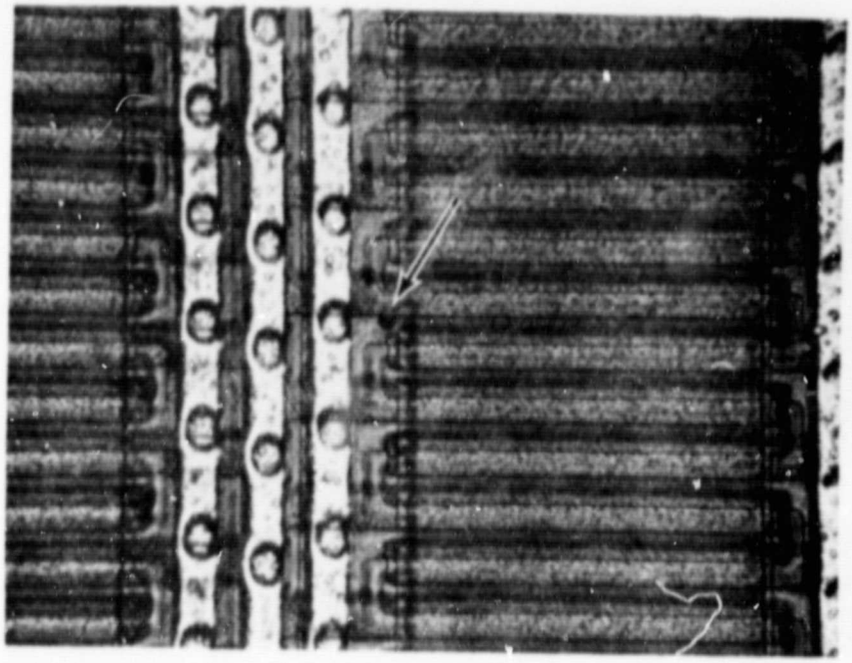


Figure IV-64 Failure Site Photograph, S/N 31, R5101; X500

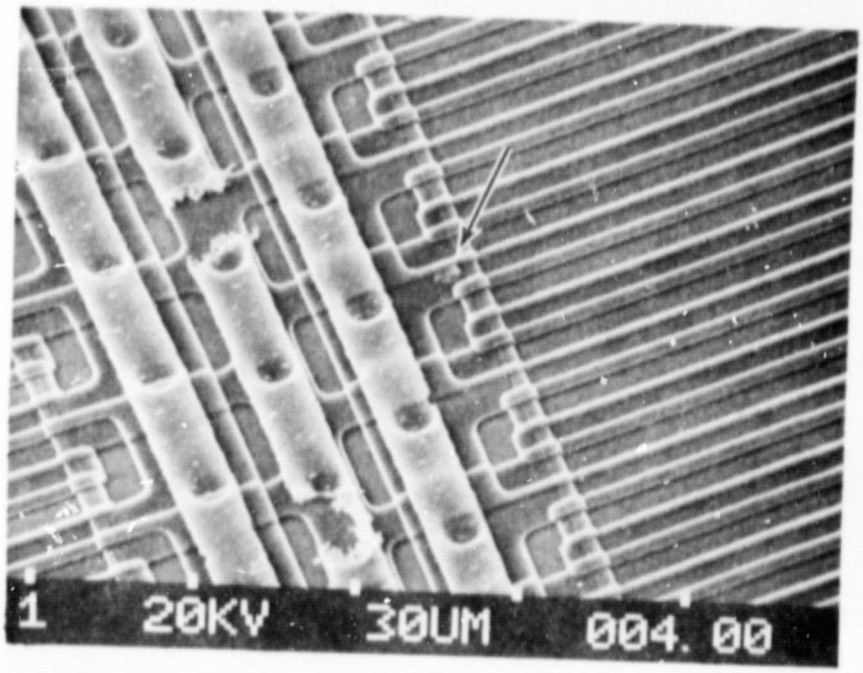


Figure IV-65 SEM Micrograph, Failure Site, S/N 31, R5101; X770

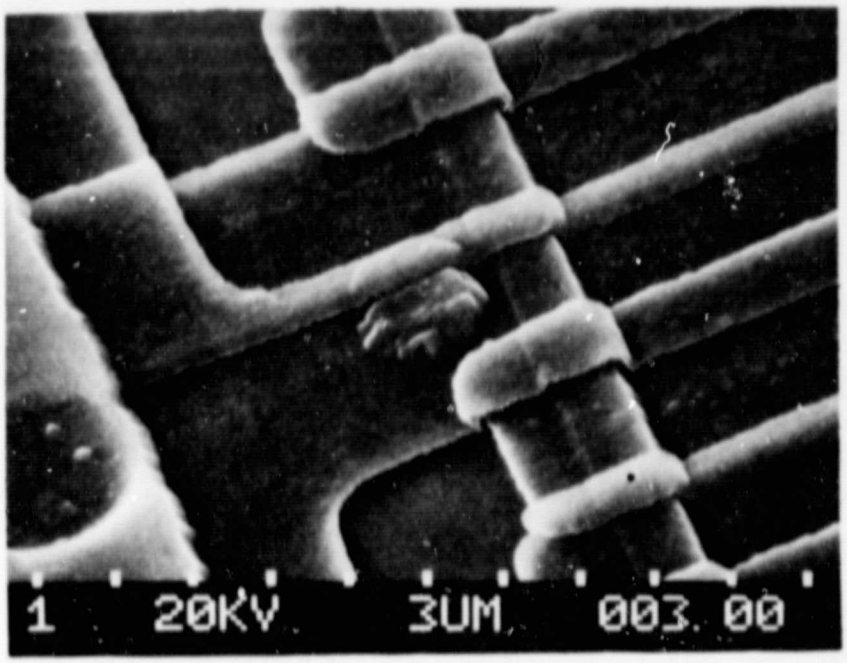


Figure IV-66 SEM Micrograph, Failure Site, S/N 31, R5101; X3700

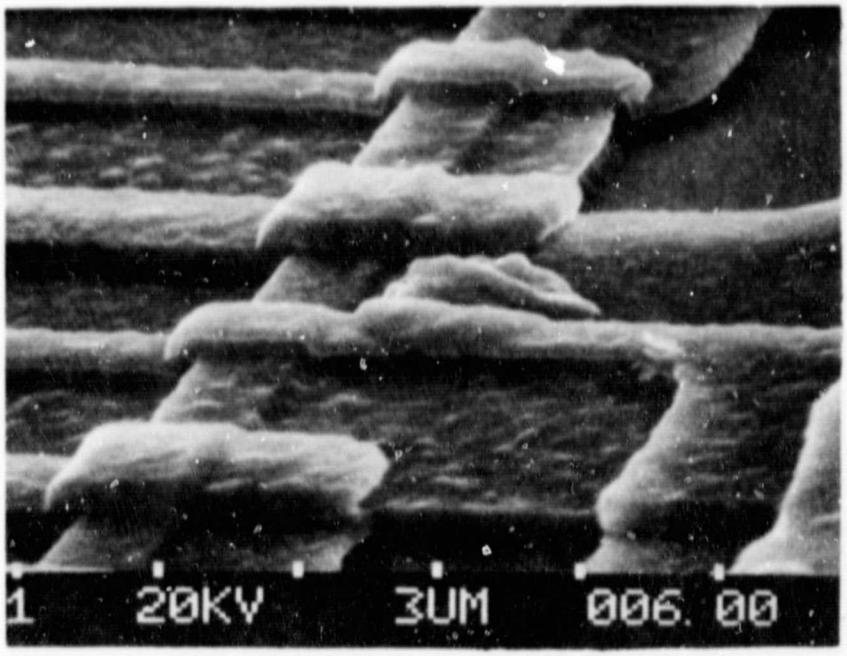


Figure IV-67 SEM Micrograph, Failure Site, S/N 31, R5101; X6500

Test Method and Disclosure: Serial number 10 was analyzed first. Pins 13, 14, and 15 were found to be leaky to pin 11. The input structure is shown in Figure IV-68. Pin 13 is identical to pin 14 except that it goes to the upper transistor in the Figure. The package was opened and the die was examined. No anomalies were noted. The input circuitry was documented and is shown in the photograph in Figure IV-69. Input pins 14 and 15 and the signal ground metallization going to pin 11 are labeled. The metallization was mechanically scribed open to isolate the input protect circiutry from the gate and from the signal ground metallization (Figure IV-70). The leakage current was isolated to the input protect circuitry. The remaining metallization was then stripped to isolate the input protect gate from the input protect source. Mechanical probing found no leakage to the transistor gate. The above analysis isolated the leakage to be related to the junctions on the input protect network. Work was then performed on serial numbers 9, 13, 21, 37, 38, and 48.

Table IV-24 lists the leakage currents measured on pins 10, 13, 14 and 15 on these units. Electrical measurement on pins 2, 3, 21 and 22 found no leakage.

The following voltage levels were on these pins during burn-in: 3-3V, 4-5V, 10-3V, 13-9V, 14-9V, 15-3V, 21-5VAC, 22-5VAC. There is no apparent relationship between the leakage current and the voltage stress. The 4 pins which had the leakage current were all along one side of the I.C. chip with pin 15 being physically closest to the output amplifier and pin 10 being the furthest away. This appears to be a contributing factor to the leakage.

The leakage current on two devices was characterized with temperature. A control unit was measured up to 180 ^{o}C and the leakage current was found to double for approximately every 10 ^{o}C increase. This part measured 104 nA at 180 ^{o}C. S/N 8 was measured up to 70 ^{o}C. The leakage on it also doubled for approximately every 10 ^{o}C increase. This reached 160 nA at 70 ^{o}C. The indication from this is that the leakage of the failures is related to junction leakage.

The conclusion is then reached that the leakage is temperature induced junction leakage.

6. R5101, S/N 38, 39, and 42

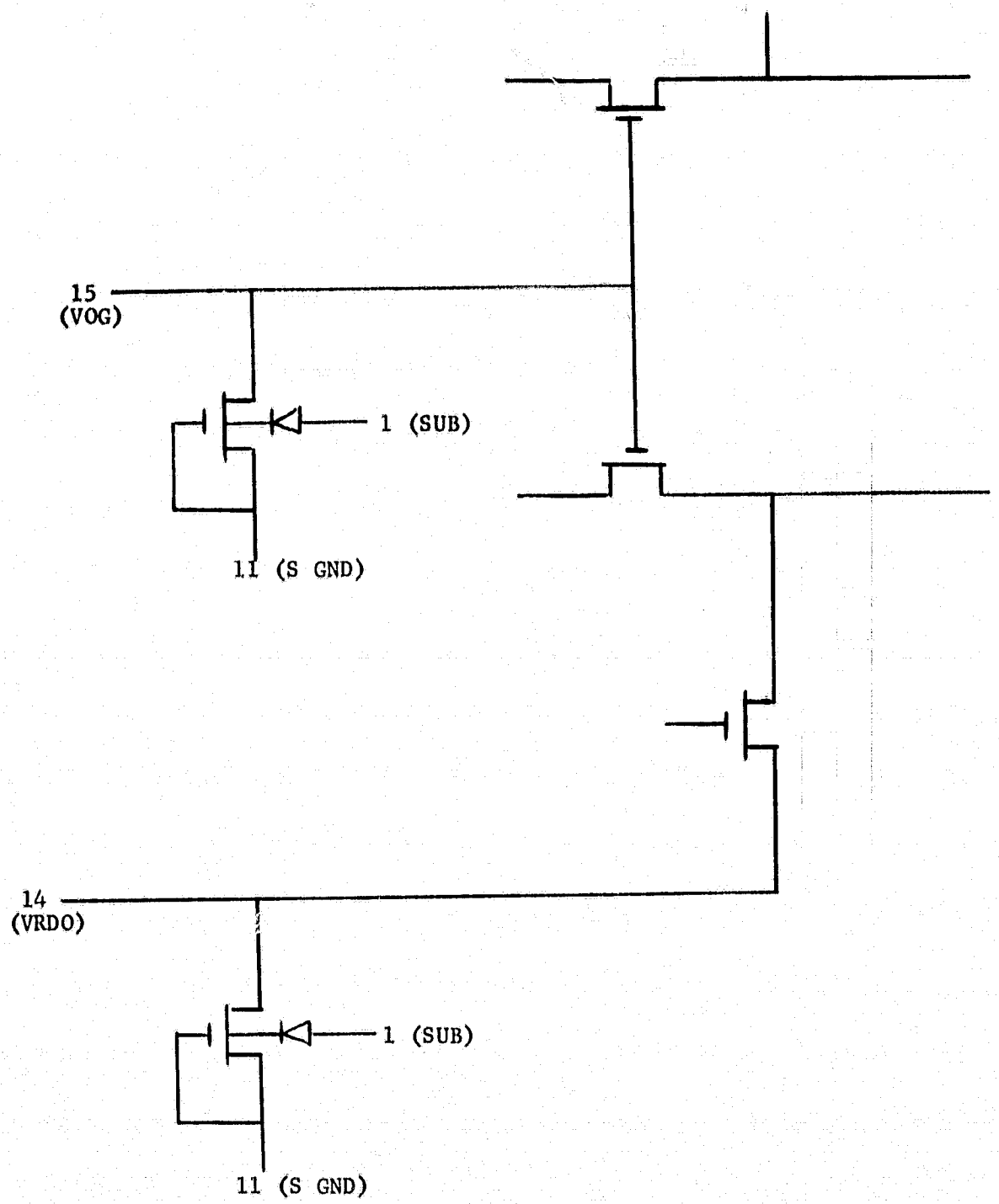


Figure IV-68 Schematic, Input Circuit, R5101

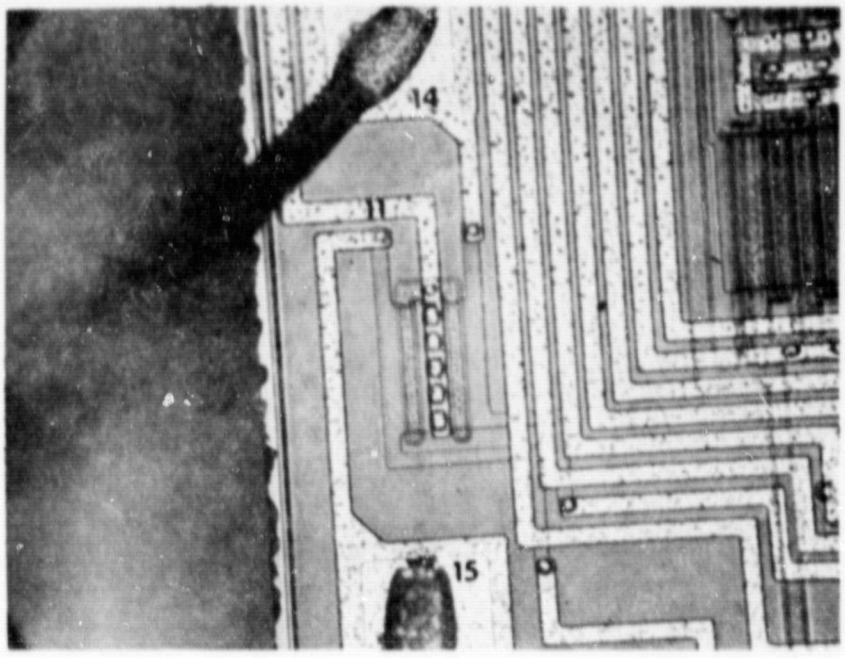


Figure IV-69 Input Protect Circuitry for Pins 14 and 15; X200

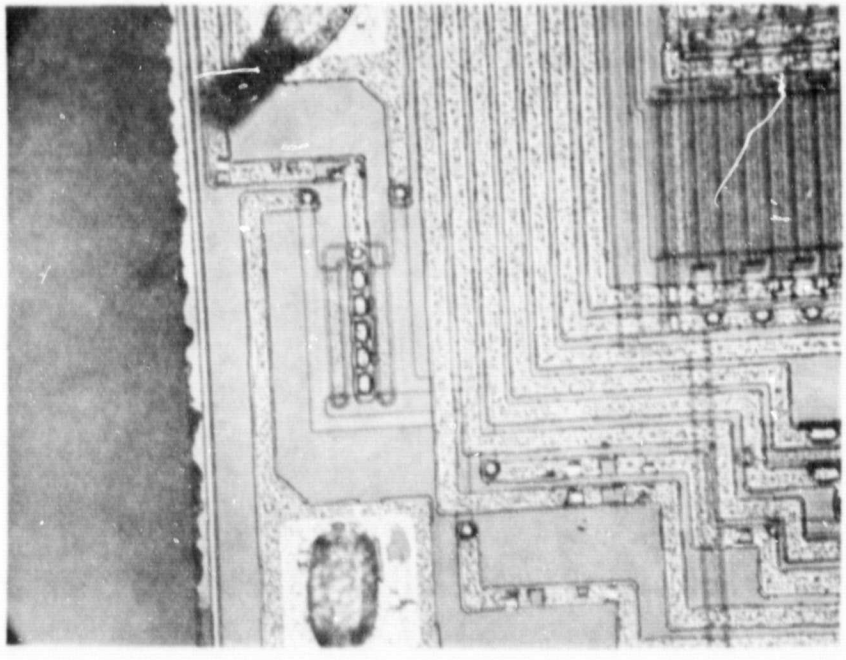


Figure IV-70 Same as Photograph 69, with Circuitry Isolated; X200

TABLE IV-24 LEAKAGE CURRENT DATA, Failure ANALYSIS, R5101

SERIAL NUMBER	8	13	21	37	38	48
PIN						
10	0	7	3	4	0	90
13	2	300	200	100	25	3
14	3	1400	1200	15	35	2
15	4	1400	300	45	50	40

ALL MEASUREMENTS IN NANOAMPERES

History: The clock current level on 43 of the 50 Reticon R5101 devices was 13 $\pm$ 1 mA. The other 7 devices had clock currents as shown below.

S/N	I_{DDC} (mA)
7	31
13	30
22	36
37	21
38	34
39	30
42	33

The cause for this higher current level was analyzed by taking voltage level measurements on S/N 7, 22, 38, 49 and 42. Serial numbers 38, 39 and 42 were then chosen for failure analysis.

Cause: The higher current levels were due to incomplete etching of the lower poylsilicon layer which created shorts between the ϕ1 and ϕ3 electrodes.

Conclusion: The lower level polysilicon is etched to form an interdigitated pattern with the "fingers" going to one side being attached to ϕ1 and the "fingers" going to the other side being attached to ϕ3. When the polysilicon is not completely etched a short results between these two gates. These were found to be typically about 500 ohms. The circuit operation did not seem to be parametrically degraded due to this condition, except for a reduction in bandwidth. These circuits had bandwidth that ranged from 50-140 KHz while the other parts were typically 160 KHz.

Test Method and Disclosure: Measurement of the ϕ3 out signal on devices which had the higher current flow found the high level to be about one volt below normal and the low level to be about one half of a volt above normal. This condition existed on the five circuits measured, S/N 7, 22, 38, 39 and 42.

Mechanical probing of ϕ3 on S/N 38 and 42 found both to be shorted to ϕ1. Voltage drop measurements along the ϕ1 metallization allowed the failure sites to be located.

The photograph in Figure IV-71 is of the short on S/N 38. This shorts the two ϕ1 electrodes to the ϕ3 electrode between them.

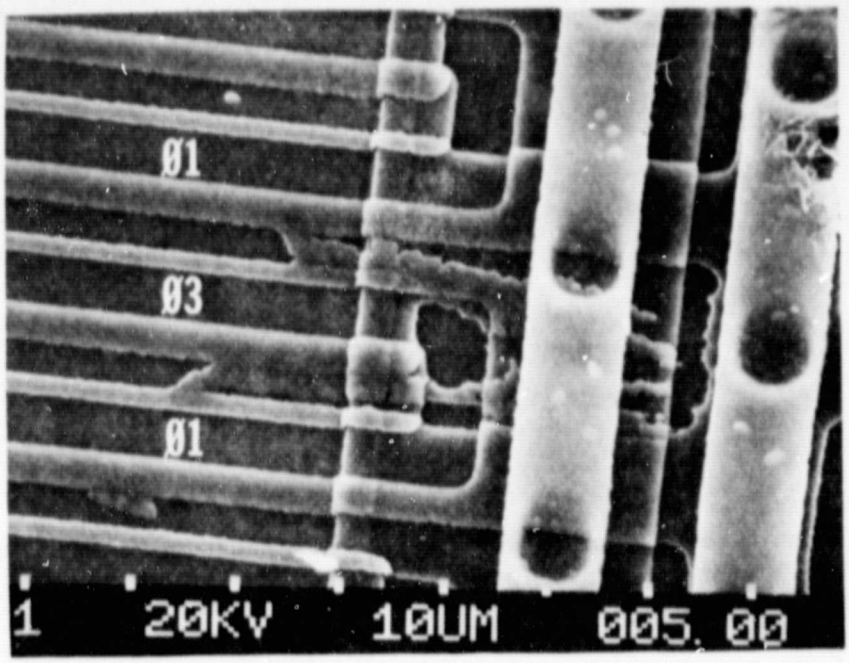


Figure IV-71 SEM Micrograph, Failure Site, S/N 38, R5101; X1400

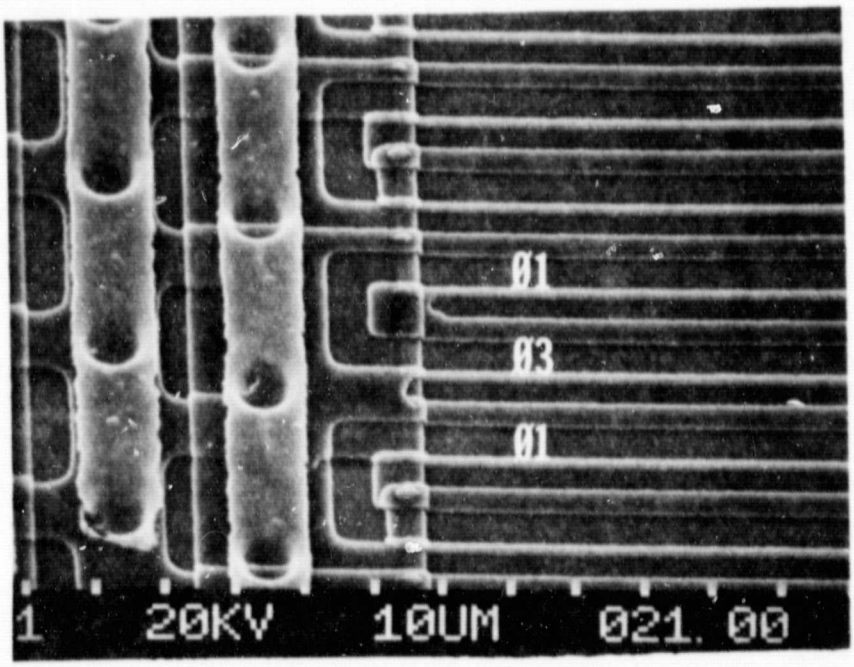


Figure IV-72 SEM Micrograph, Failure Site, S/N 42, R5101; X1000

The photograph in Figure IV-72 is of the short on S/N 42. This produces the same type of short as on S/N 38. The $\phi 3$ electrode coming from the right hand side does not terminate like the gates above and below it. It is continuous and connects $\phi 3$ to $\phi 1$.

S/N 39 was opened and a small drop of temperature sensitive nematic liquid crystal was placed on the surface. Power was then applied to the device using a curve tracer and the failure site was observed (Figure IV-73). The change in alignment of the liquid crystals allows the current path to be visible. Figure IV-74 shows this same area with the liquid crystal removed. The current flowed from $\phi 1$ to $\phi 3$ via the polysilicon connecting the two in the middle.

All three failure modes were identical and were due to a masking or etching defect.

K. Conclusions and Recommendations

This section will address the objectives established for this study and provide a summary of the results.

1. Design Strengths and Weaknesses

The R5101 has an on-chip clock generator and driver circuit. This eliminates timing difficulty associated with external phase clocks. The voltage level required is only 5 volts for the square wave clock input. This is in contrast to 13-15 volt clocks required on the CCD321A.

With an on-chip generator the phase relationship between the clock input and the four clock drivers has to be established by a separate sync clock input. This requires the development of the proper timing for this input if synchronous operation is required.

The R5101 has two output signals, however, one is only delayed one-half of a sample time from the other and is identical in magnuitude. These two signals can be summed by using an adder circuit. This does not change the available bandwidth capability since the sampling frequency is set by $\phi 2$.

The transfer function on the R5101 produces a low output for a high input and vice-versa. This may cause some confusion for the user.

The R5101 is manufactured utilizing the surface channel charge coupled device technology. The transfer efficiency and bandwidth were found to be lower for this technology than for the Buried Channel CCD. The transfer efficiency is still very high and is not likely to create a problem for most applications. The bandwidth was on the order of 160 KHz.

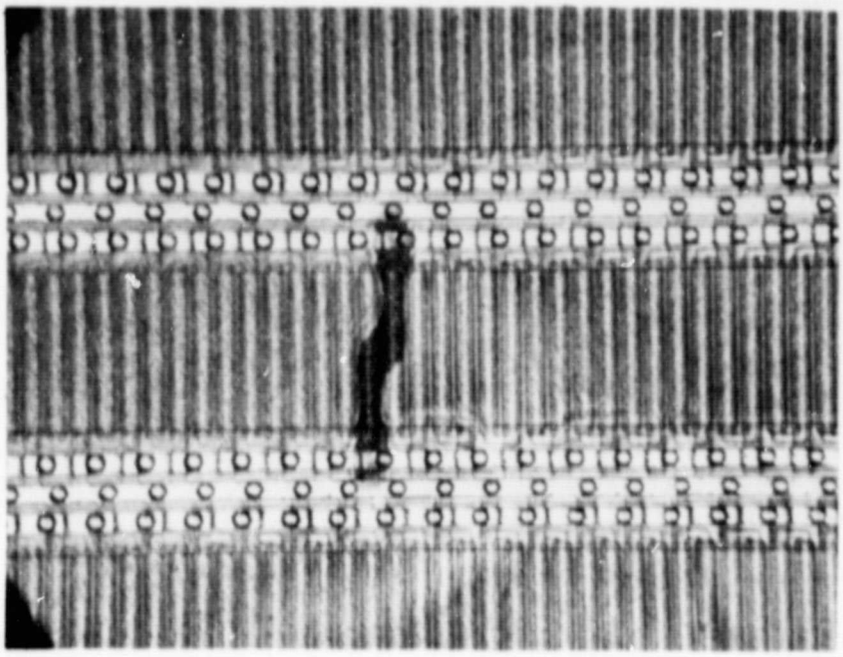


Figure IV-73 Failure Isolation Using Liquid Crystals; X200 S/N 39

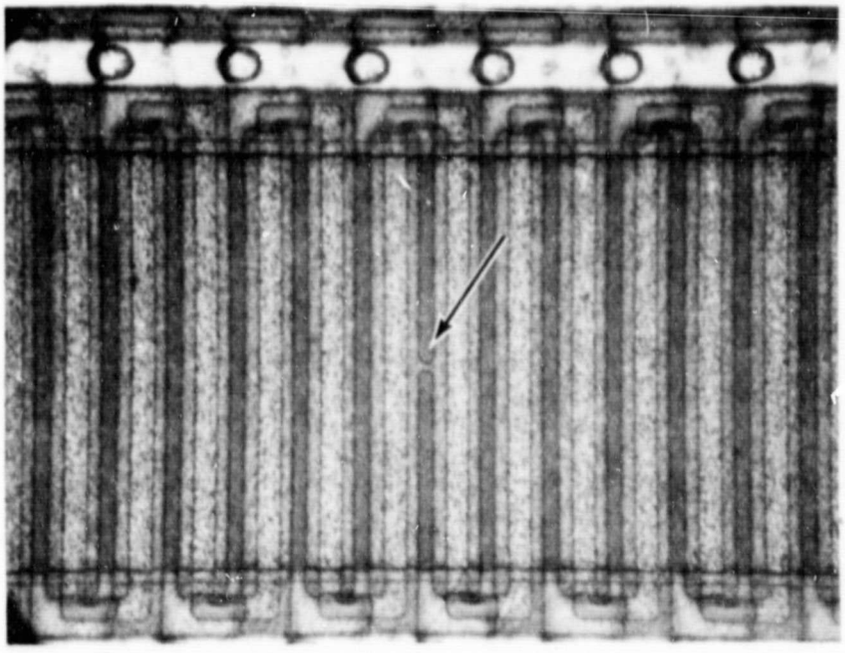


Figure IV-74 Failure Site Photograph, S/N 39, R5101; X500

2. Failure Modes

The R5101 utilizes MOS structures and therefore require special handling relative to electrostatic sensitive parts. Two devices were received with damaged gates on the sync input. It is likely that this input is not properly tested prior to shipping of the parts since it is not required to test functionality. An input leakage test should be performed by the vendor or at incoming test.

Current paths between the two polysilicon layers and between adjacent electrodes in the same layer are also a prominent failure mode. Two conditions were found to cause this on these parts. One part had a large increase in clock current due to a particle within the shift register section which resulted in a current path between two clock electrodes, one a poly1 electrode and the other a poly2 electrode. Incomplete etching of the first polysilicon layer created high current conditions on 7 devices due to current paths between the ∅1 and ∅3 clocks. These parts can be detected by their abnormally high clock current or their low bandwidth. The remainder of the parameters showed little difference.

Several devices developed low level leakage on the input protect structure with operating life. This is not considered to be a reliability concern as it is unlikely to cause device failure with normal operating life.

3. Parametric Measurements

The manufacturers data sheet consists primarily of a list of operating conditions at this time. The only performance parameters listed are clock current and gain. The following parametric measurements would have adequately screened the defective and marginal parts received and are therefore recommended for use in future procurement:

a. Device Power - A high reading of clock current indicates a probable short within the clock circuitry or the shift register electrodes from Table IV-20 it is recommended that this value be 15 mA at 25 °C under the test conditions specified therein. This value is about 5.4 standard deviations above the mean value of 13.12 mA in Table IV-20. Thus indicating the probability of rejecting a good part is extremely low, less than .00001%. All "bad" parts would be rejected and were much greater than 15 mA.

b. Input Gate Leakage - Leakage to a MOS input indicates a degraded structure. All good parts tested was less than 0.1 microamps at 25°C.

c. Operating Point - This test would verify that the device will work with the input range required. This can be performed by monitoring the output waveform resulting from a low frequency sine wave input. The good devices which successfully performed under high stress test passed an initial test of 1.0 volts peak to peak operating around a 4.5 volt d.c. input, (VIC = 3.0V).

d. Gain - This parameter should be measured in conjunction with the operating point. It is recommended that a minimum value of 0.5 be specified with an input per para. c above. Again, this value is about 5.4 standard deviations from the side 1 mean value of Table IV-20. (Side 2 is 6.4 standard deviations.)

e. Bandwidth - The bandwidth, or a test to verify the functionality of the device at the desired operating frequency should be performed. This type of test is a necessity since the remainder of the parameters could be acceptable but due to manufacturing variations some of the parts may not work at higher frequencies. The manufacturer's specification of 12.5% of the sampling frequency should be used. At a 1 MHz sampling frequency, good parts will have a bandwidth greater than 125 KHz.

4. Burn-In Circit

The burn-in circuit utilized for this study provides dynamic operation of these circuits. A simpler circuit will be adequate. This would consist of the circuit of Figure IV-58 except the sync input timing is not required.

5. Changes to Upgrade Reliability

These circuits are very temperature sensitive and operate in a limited temperature range. The parts operate very reliably in the range of -25 ^{o}C to +55 ^{o}C when screened as recommended herein. These limitations are inherent in the devices, themselves and no recommendations can be made at this time to improve performance in this respect. However, these parts are not damaged by operation at temperatures up to 125 ^{o}C and even greater. Additional characterization to determine performance parameters and operating limitations at higher temperature will yield data which may be useful in specific applications.

6. Screening Recommendations

The electrical screening should be as discussed in para. 3 above Environmental screening was performed per MIL-STD-883, Method 5004. The results of the life test indicates that this was adequate to provide reliable devices. The parts do not

degrade due to exposure to temperature extremes of -65 °C to +150 °C. The 160 hour burn-in was performed at 55 °C. No maximum operating temperature was specified in the manufacturer's data sheet. 55 °C was utilized since this was the maximum temperature specified for the CCD321A and this was the temperature used for the 160 hour burn-in on that device. The results of this study indicate that this can be increased to the 125 °C level specified in Method 1015.

7. Application and Derating Guidelines

The R5101 is an analog delay line intended for audio signal-delay applications. Some of these applications were discussed in the introduction. New applications are being developed as the technology progresses.

There was no evidence that device derating is required. The outputs were operated for the 4000 hour life test at 2000 ohm loading with no adverse effects.

8. Degradation of Charge Transfer Efficiency with High Temperature Operation

There was no evidence of a decrease in the transfer efficiency with operation at up to 185 °C. These parts are limited to operating temperatures well below this point so this mechanism is not expected to be a factor in the operation of these circuits.

V. FAIRCHILD CCD321A-2

A. Physical Construction

The CCD321A-2 is a buried channel CCD. The following section will discuss its construction. This will include physical dimensions and type of package, residual gas analysis, C-V curves, circuit schematics, microsections, and examination of the individual layers on the die.

1. Package

The CCD321A-2 is in a 16 pin ceramic dual-in-line package (Figure V-1). This is a multilayer side braze construction with a braze sealed metal lid. Pin 1 is marked by a B on top of the ceramic. The metal lid is electrically connected to pin 8, V_{SS}. There are 8 leads on each side of this package at 0.1 inch spacings. The package width is 0.3 inches. The serial number was placed on the package to keep device identity during the course of the testing.

2. Residual Gas Analysis

The RGA was performed as discussed in the R5101 section. The CCD321A-2 package is smaller than the Reticon package with an internal volume of approximately 0.05cc. This is an adequate quantity of gas to do an analysis and created a pressure rise of 125 microns within the puncture tool.

The table below lists the gases detected and their mole percentages:

Gas	S/N 17	S/N 0
Nitrogen N_2	99.26	99.35
Oxygen O_2	.50	.17
Water H_2O	<.01	<.01
Carbon Dioxide CO_2	.16	.37
Methane CH_4	.04	.07
Argon Ar	.03	.03

This is an acceptable gas ambient and does not represent a reliability concern for this device.

Figure V-1 Package, CCD321A; 5X

3. Capacitance Versus Voltage Plots

The physics of the analysis of C-V curves was covered in the R5101 section and will not be repeated here. On the CCD321A the C-V plots were taken between pins 3 and 5 and pins 12 and 13. This was performed on serial numbers 8 and 45. Pin 3 = V_{IA}, Pin 5 = ϕ_{SA}, Pin 12 = V_{RB}, and Pin 13 = V_{IB}. These pin combinations allowed for C-V plots to be made without the need for mechanical probing of the chip. ϕ_{SA} and V_{RB} are gates and V_{IA} and V_{IB} are contacts to n-type material beneath these gates.

The shift in the transition point ranged from 0.15 volts to 0.6 volts. The thickness of the oxide in this area was estimated to be approximately 800 Angstroms. The range of values for Q_o/q is shown in the following equations:

$$\Delta V = 0.15 \text{ to } 0.6$$

$$\Delta V = \frac{Q_o}{C_o}$$

$$\frac{Q_o}{q} = \frac{\Delta V C_o}{q}$$

$$C_o = \frac{K_o \epsilon_o}{X_o} = \frac{(3.9)(8.86 \times 10^{-14} \text{ F/cm})}{800 \times 10^{-8} \text{cm}}$$

$$C_o = 4.32 \times 10^{-8} \text{F}$$

$$\min \frac{Q_o}{q} = \frac{(.15)(4.32 \times 10^{-8} \text{ F})}{1.6 \times 10^{-19} \text{ coulombs}} = 4 \times 10^{10}$$

$$\max \frac{Q_o}{q} = \frac{(.60)(4.32 \times 10^{-8} \text{ F})}{1.6 \times 10^{-19} \text{ coulombs}} = 1.6 \times 10^{11}$$

These values are in an acceptable range of mobile ion charge density. The readings are shown in Table V-1 and the curves are drawn in Figures V-2 thru V-5. The parts were biased at 15 volts and heated to 300°C for 10 minutes. They were then allowed to cool down under bias and the C-V readings taken.

TABLE V-1a C-V PLOT DATA, S/N 8; 321A

10 MIN, 300°C, 15 V			ANNEALED		10 MIN, 300°C, 15 V			ANNEALED	
CAPAC pF	NORMAL-IZED	DC BIAS	CAPAC pF	NORMAL-IZED	CAPAC pF	NORMAL-IZED	DC BIAS	CAPAC pF	NORMAL-IZED
.7048	.9969	5	.7016	1.0	.8050	1.0	5	.7914	1.0
.7054	.9977	4	.6962	.9923	.8014	.9955	4	.7866	.9939
.7070	1.0	3	.6930	.9877	.7970	.9901	3.8	.7824	.9886
.7050	.9972	2	.6930	.9877	.7892	.9804	3.6	.7750	.9793
.7050	.9972	1	.6924	.9869	.7626	.9473	3.4	.7634	.9646
.7050	.9972	0.8	.6924	.9869	.7316	.9088	3.2	.7442	.9403
.7060	.9986	0.6	.6900	.9835	.7156	.8889	3.0	.7210	.9110
.7050	.9972	0.4	.6860	.9778	.7144	.8874	2.8	.7056	.8916
.7040	.9958	0.2	.6744	.9612	.7132	.8860	2.6	.7010	.8858
.7030	.9943	0	.6728	.9590	.7154	.8887	2.4	.7014	.8863
.6930	.9802	-0.2	.6732	.9595	.7160	.8894	2.2	.7026	.8878
.6856	.9697	-0.4	.6706	.9558	.7172	.8909	2.0	.7030	.8883
.6836	.9669	-0.6	.6696	.9544	.7194	.8937	1.0	.7056	.8916
.6825	.9653	-0.8	.6690	.9535	.7216	.8964	0	.7100	.8971
.6818	.9644	-1	.6700	.9550	.7162	.8897	-1	.7034	.8888
.6800	.9616	-2	.6680	.9521	.7134	.8862	-2	.7014	.8863
.6772	.9578	-3	.6656	.9487	.7116	.8840	-3	.6994	.8837
.6764	.9567	-4	.6654	.9487	.7112	.8835	-4	.6984	.8825
.6770	.9576	-5	.6644	.9470	.7096	.8815	-5	.6970	.8807

TABLE V-1b C-V PLOT DATA, 45, 321A

10 MIN, 300°C, 15 V			ANNEALED		10 MIN, 300°C, 15 V			ANNEALED	
CAPAC pF	NORMAL-IZED	DC BIAS	CAPAC pF	NORMAL-IZED	CAPAC pF	NORMAL-IZED	DC BIAS	CAPAC pF	NORMAL-IZED
.6886	1.0	5	.5924	1.0	.7792	1.0	5	.7160	1.0
.6854	.9954	4	.5872	.9912	.7772	.9974	4	.7078	.9886
.6784	.9852	3	.5861	.9894	-	-	3.5	.6804	.9503
.6754	.9808	2	.5841	.9860	.7488	.9610	3	.6562	.9165
.6735	.9781	1	.5836	.9851	.7332	.9410	2.8	-	-
.6744	.9794	0.6	-	-	.7166	.9197	2.6	-	-
-	-	0.5	.5716	.9649	-	-	2.5	.6444	.9000
.6660	.9672	0.2	-	-	.7040	.9035	2.4	-	-
.6472	.9399	0	.5556	.9379	.7003	.8987	2.0	.6408	.8950
.6440	.9352	-1	.5534	.9342	.7016	.9004	1.0	.6400	.8939
.6414	.9315	-2	.5524	.9325	.6990	.8971	0	.6398	.8936
.6404	.9300	-3	.5503	.9289	.6980	.8958	-1	.6376	.8905
.6394	.9286	-4	.5492	.9271					
.6382	.9268	-5	.5462	.9220					

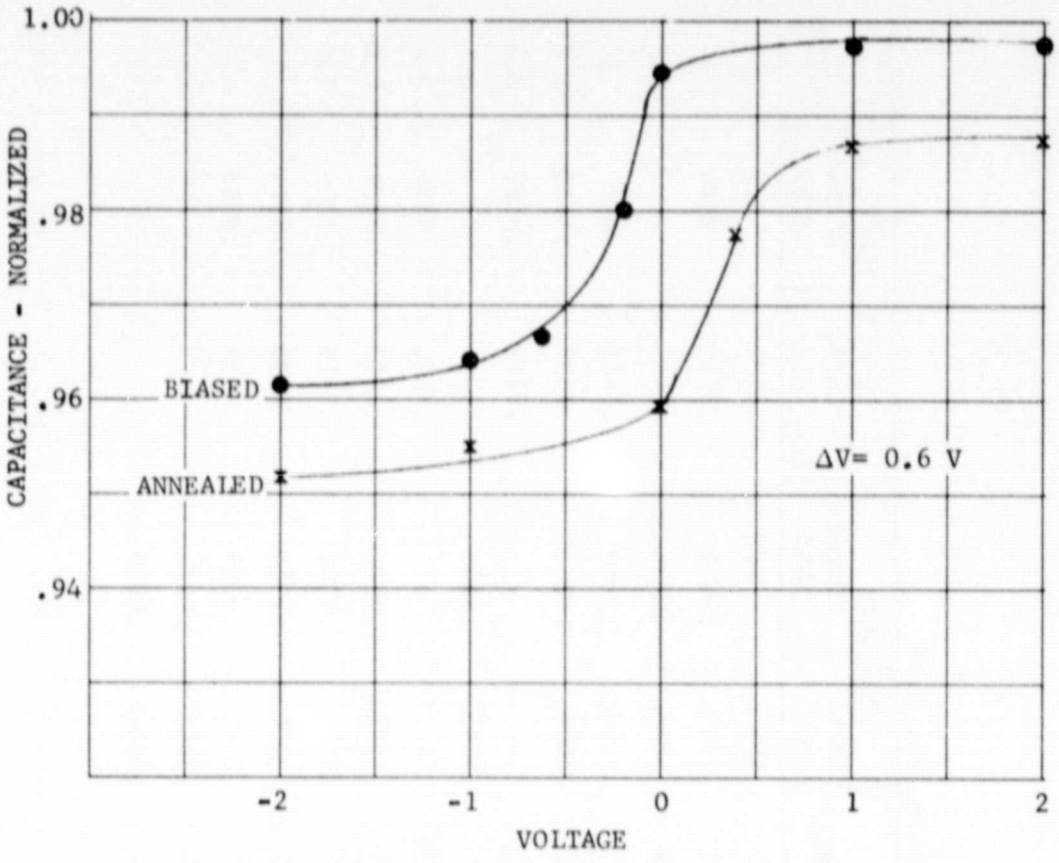


Figure V-2 C-V Plots, S/N 8, Pins 3-5, CCD321A

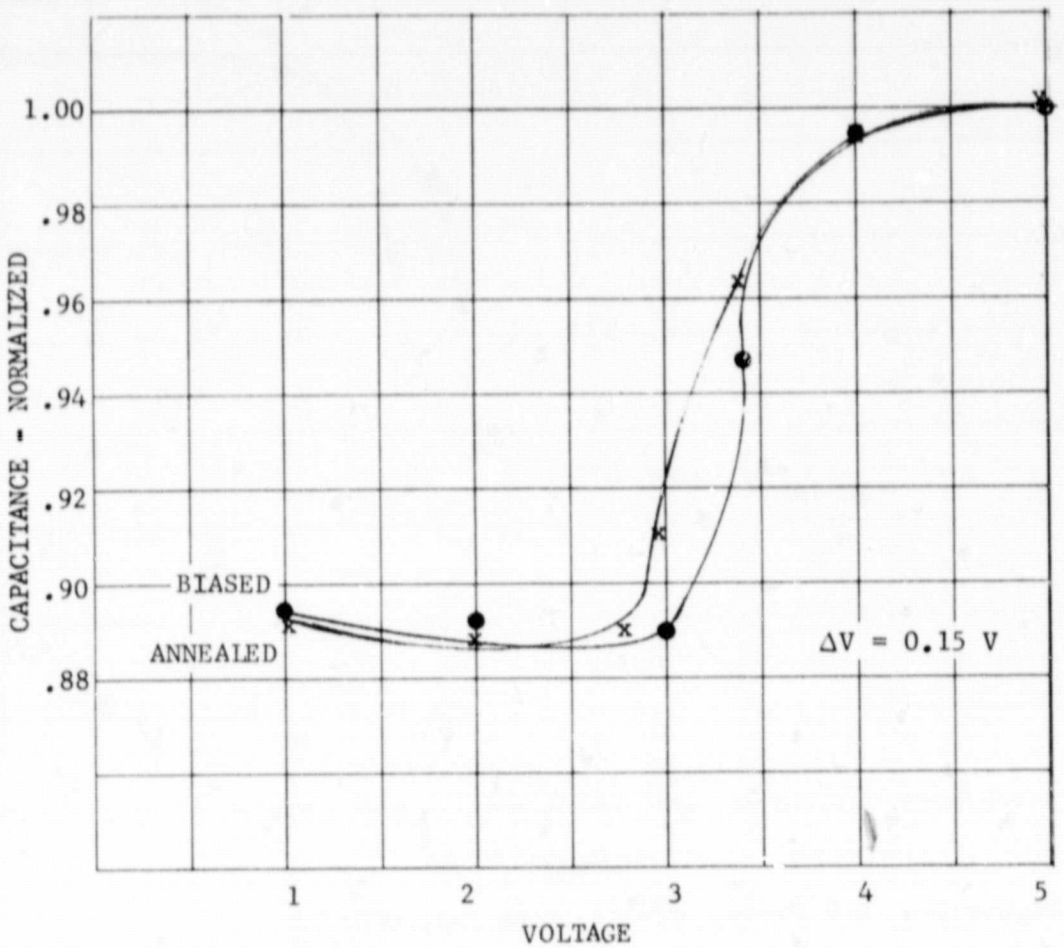


Figure V-3 C-V PLOTS, S/N 8, Pins 12-13, CCD321A

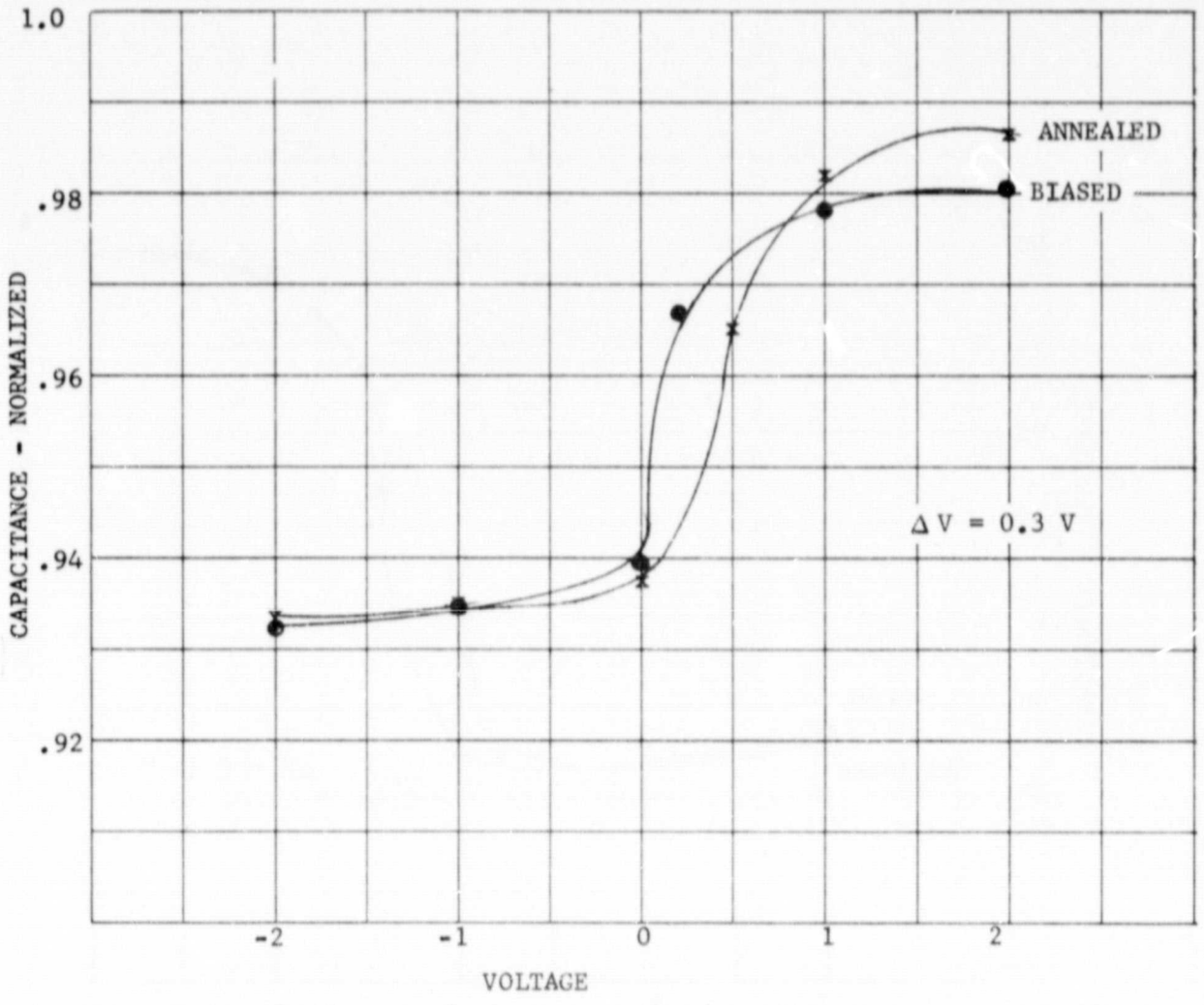


Figure V-4 C-V Plots, S/N 45, Pins 3-5, CCD321A

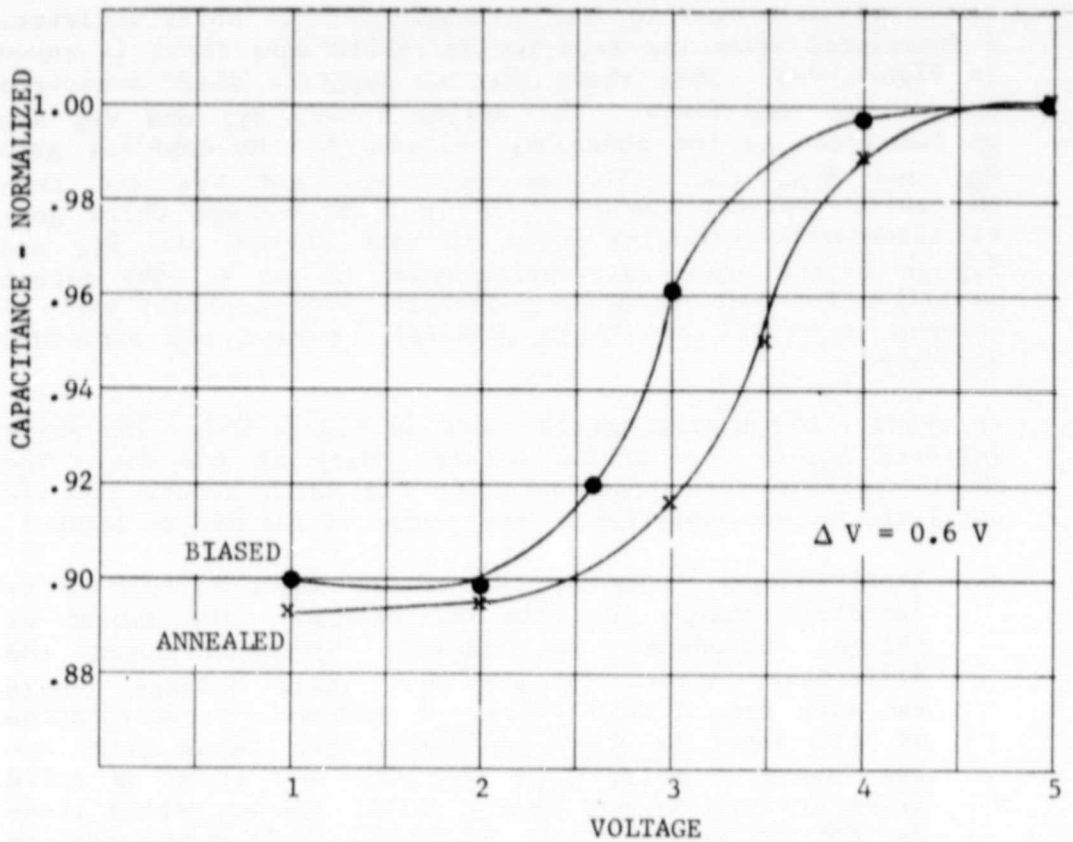


Figure V-5 C-V Plots, S/N 45, Pins 12-13, CCD321A

They were then annealed at 300 °C for 10 minutes without bias and the final readings taken. From the Figures it is evident that the transition point for the pin 3-5 measurement is different than that for the pin 12-13 measurement. This is the work function difference between the two polysilicon layers. Pin 5 is connected to the poly1 layer and pin 12 is connected to the poly2 layer. There is approximately three volts difference in this flatband voltage and this provides the directionality associated with charge movement in the channel as will be discussed in the following section.

4. Schematic

The CCD321A is a 455/910 bit analog shift register. It contains two separate 455-bit shift registers which can be connected in series to form a single 910-bit shift register. A functional schematic from the Fairchild data sheet is shown in Figure V-6. This shows the two separate shift registers and output amplifiers. The analog inputs V_{IA} and V_{IB} are on the input to the channels, followed by the sampling gate ϕ_{SA} and ϕ_{SB}, the reference gate V_{RA} and V_{RB} and then the shift register channel. V_2 is a DC voltage which goes to alternating pairs of gates in each channel and ϕ_{1A} and ϕ_{1B} go to the other alternating pairs of gates. The output amplifier for both sides is identical. The sections will be covered in detail and their physical location and structure discussed.

An overall die photograph is shown in Figure V-7. The shift register inputs are on the outside edges of the die. The shift register then traverses back and forth across the die until the output amplifier in the center of the die is reached.

a. Input Circuit - The purpose of the input circuit is to introduce charge into the CCD channel. The amount of charge introduced is linearly dependent upon the difference between V_I and V_R. These voltage levels can vary from 3 to 7 volts. A schematic representation of this input is shown in Figure V-8. Since there are two layers of polysilicon the gates are shown as solid lines for the bottom layer, poly1, and as dotted lines for the top layer, poly2. A cross-section representation of this is shown in Figure V-9. Below the cross-section is a representation of the potential wells produced beneath the gates. A photograph of this area is shown in Figure V-10. At time T1 with ϕ1 high, there is charge present beneath the ϕ1 gate electrodes. The cascade effect is produced by the work function difference of the poly1 and poly2 layers. V2 is at a fixed potential of about 7.5 volts while ϕ1 goes from 0 to 15 volts. This produces the stair step condition seen with either ϕ1 having the deepest well (T1) or V2 having the deepest

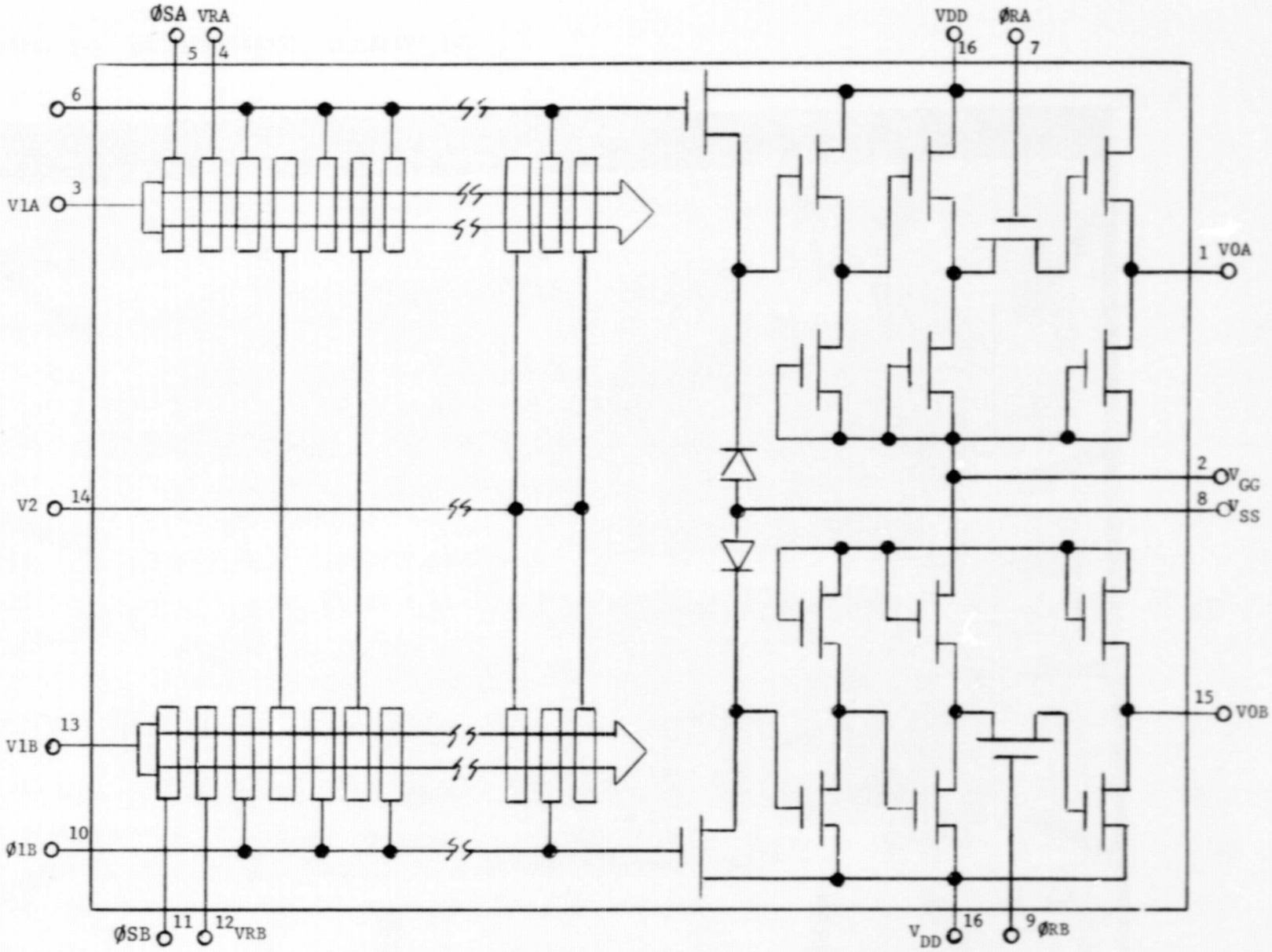


Figure V-6 Functional Schematic, CCD321A

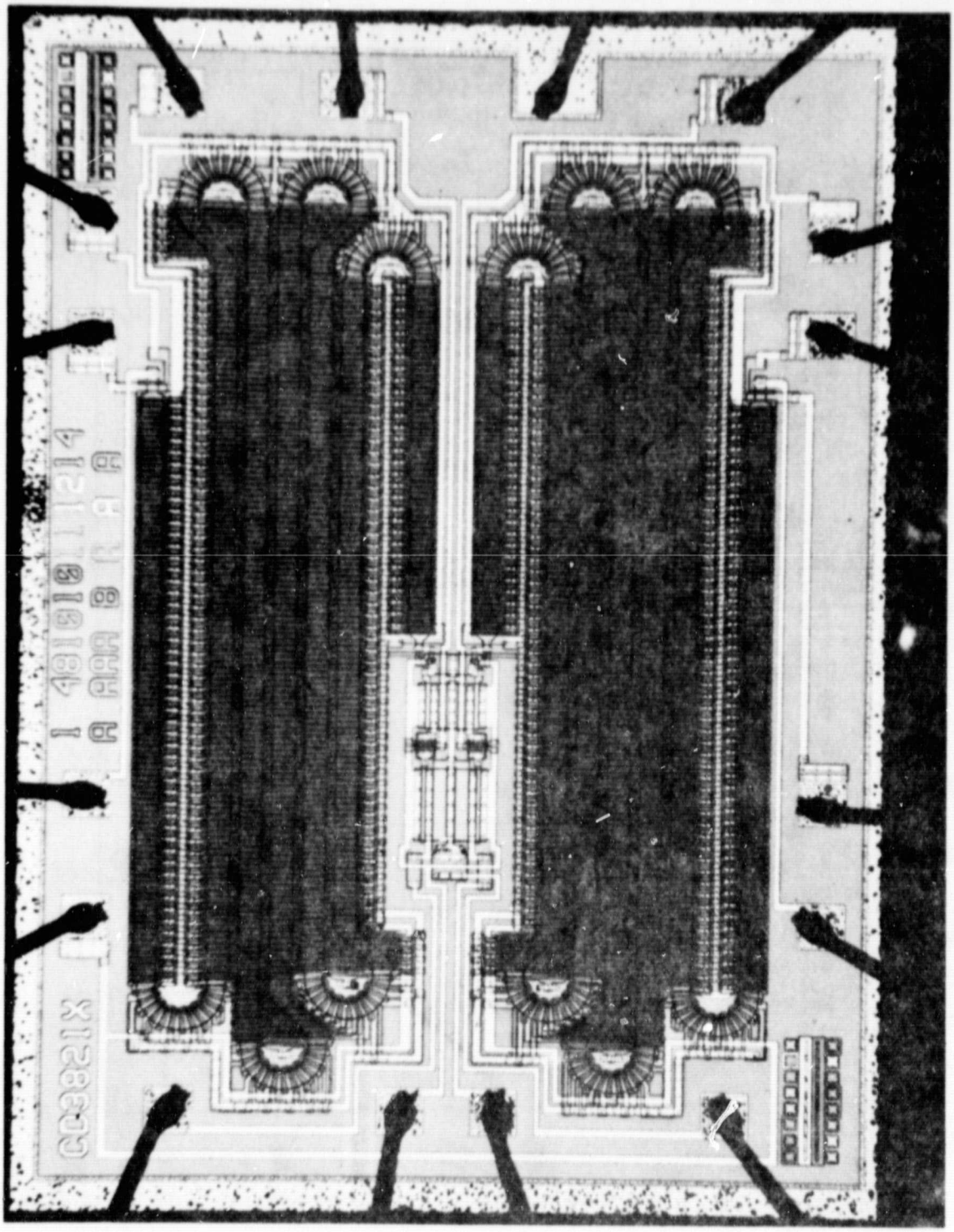


Figure V-7 Die Photograph, CCD321A; X60

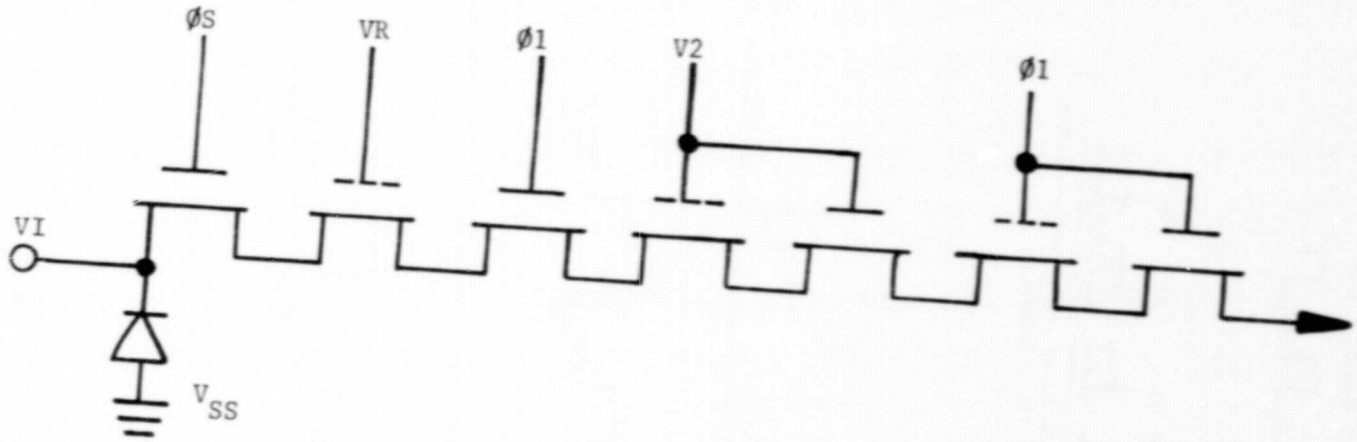


Figure V-8 Schematic, Input, CCD321A

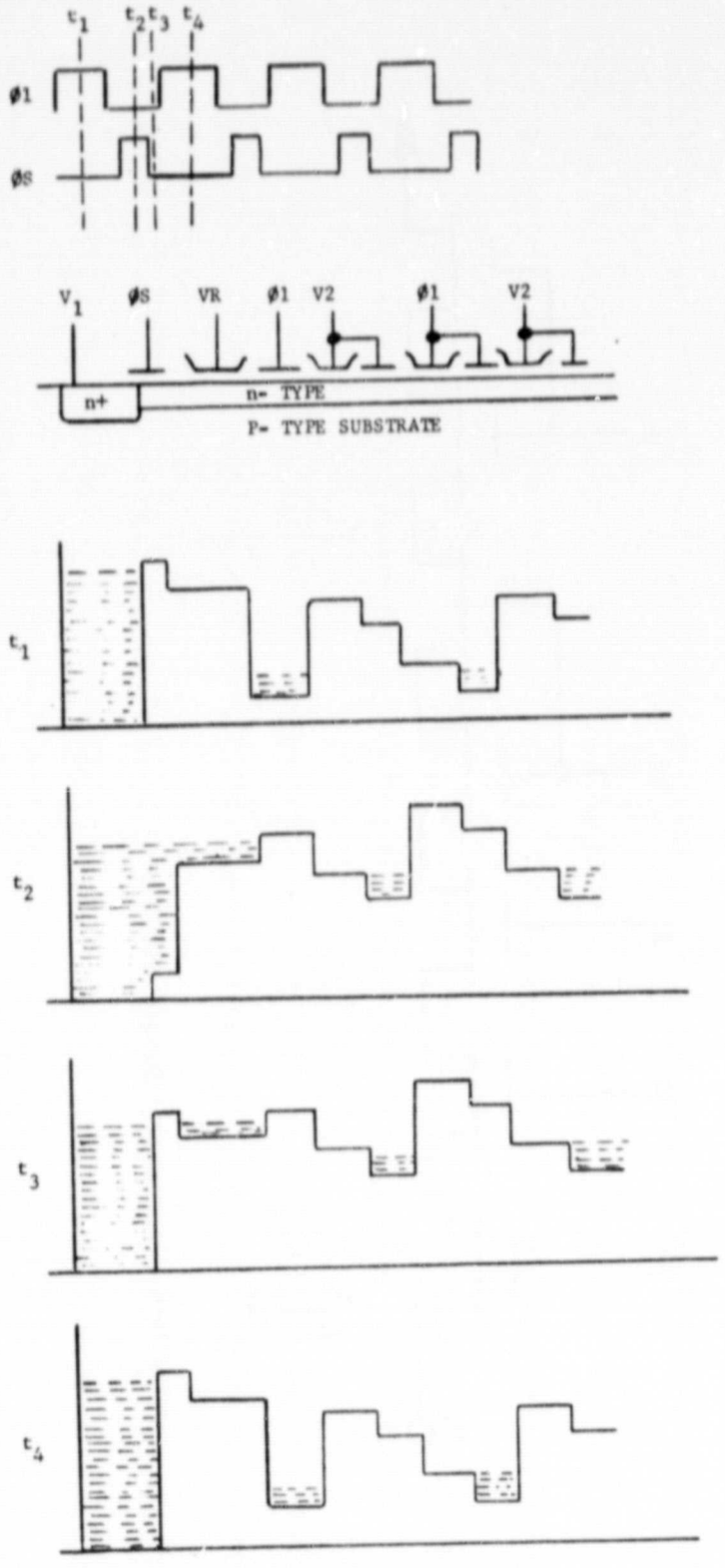


Figure V-9 Input Timing, Cross Section and Potential Wells, CCD321A

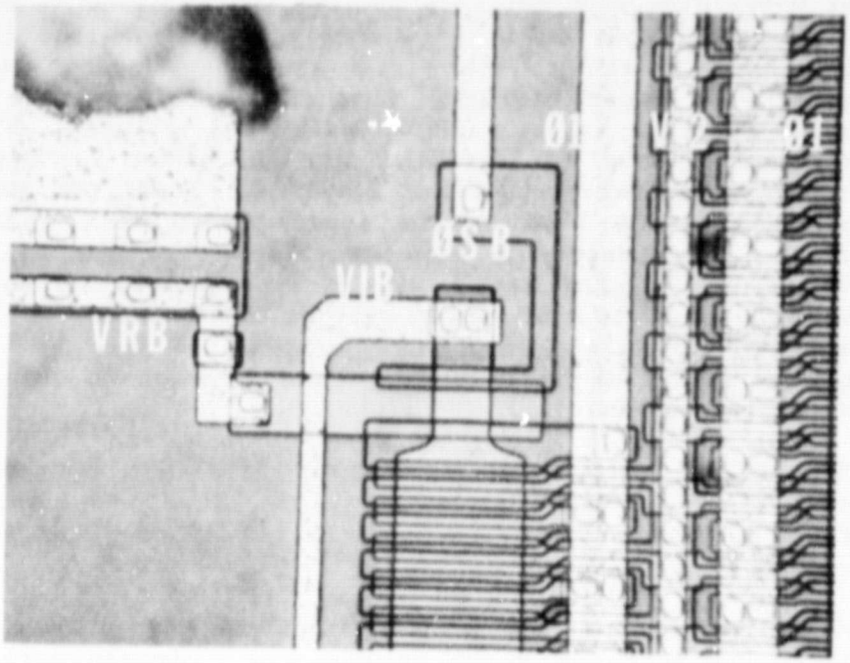


Figure V-10 Input Circuitry, CCD321A; 500X

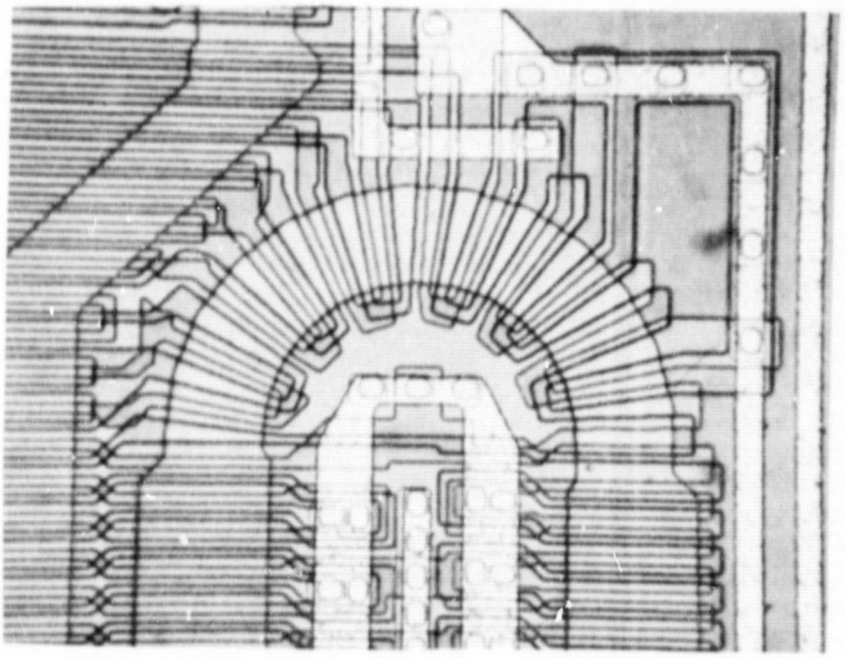


Figure V-11 Corner Structure, CCD321A; 500X

well (T2). At time T2 the charge which was beneath the ØI poly1 electrode moves to the area beneath the V2 poly1 electrode. Also at this time ØS goes high which allows the input charge to move into the area beneath the V_R gate. The amount of charge which is introduced into the shift register is then controlled by two voltages. These voltages control the depth of the well under V_R, with a higher potential producing a deeper well, and the amount of the reverse bias on the input diode, with a lower reverse bias supplying more electrons. In the Figure, V_R is at 6 volts and V_I is at approximately 3 volts. When ØS goes low the sample will be locked into the area under the V_R electrode. This is shown at time T3. The charge will then be transferred into the shift register when ØI goes high (T4).

This Figure then shows how the input signal is sampled each time ØS is high, and that the ØI clock with the fixed V2 electrodes, transfers the charge down the shift register.

b. Shift Register - The structure of the gates over the shift register was shown in the input circuit section. The V_2 and ØI electrode pairs alternate the entire length of the channel. A portion of the shift register including the corner structure is shown in Figure V-11.

c. Output Amplifier - The output amplifier is shown in the schematic in Figure V-12 and in the photographs in Figures V-13 and V-14. Figure V-13 shows the overall amplifier section. Figure V-14 shows the interface between the channel and the output. A cross-sectional view of the interface between the shift register and output amplifier is shown in Figure V-15. This shows the V_2, ØI, V_2 electrodes which transfers the charge into the n+ source diffusion of transistor Q1. This diffusion is precharged when ØI goes high. The amplifier section is more complicated than that of the R5101. Transistors Q3, Q5, and Q10 are resistive components to ground. Transistors Q6 and Q8 are always biased on and therefore are series conductors. The charge which reaches the source diffusion of Q1 will decrease the conductivity of Q2 which lowers the voltage to the gate of Q4. This decreases the conductivity of Q4 and thus lowers the voltage level that is tranferred to the gate of Q9 when ØR is high. The output voltage will decrease when the input voltage decreases and increase when the input voltage increases. The amount of charge transferred is inversely related to the input voltage level.

The transistors in this section are depletion mode field effect transistors.

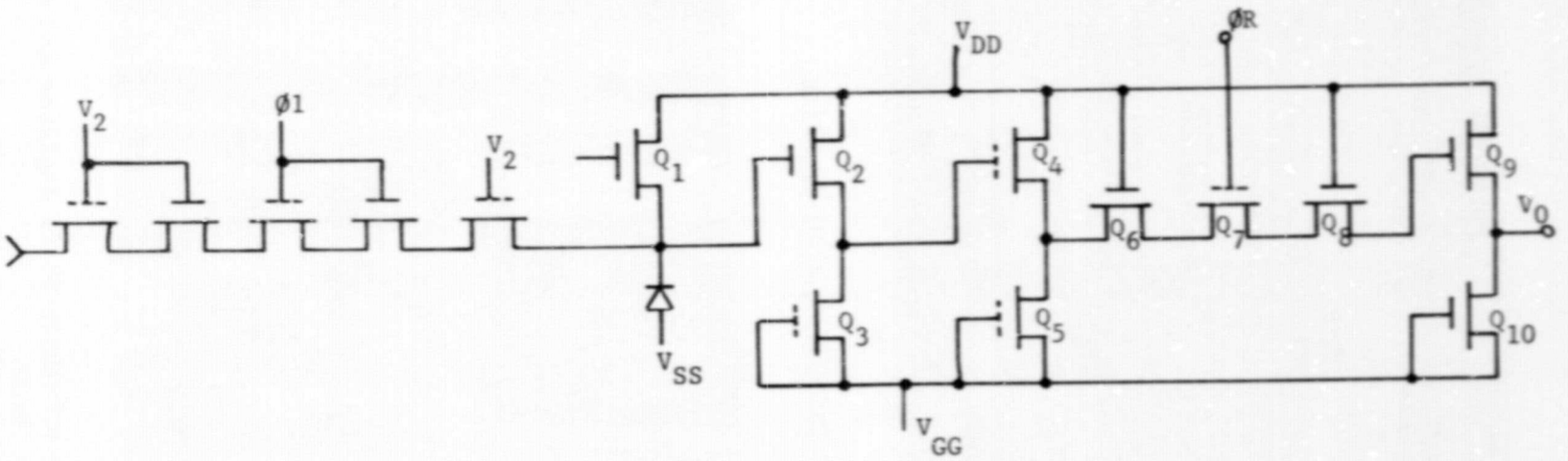


Figure V-12 Schematic, Output Circuit, CCD321A

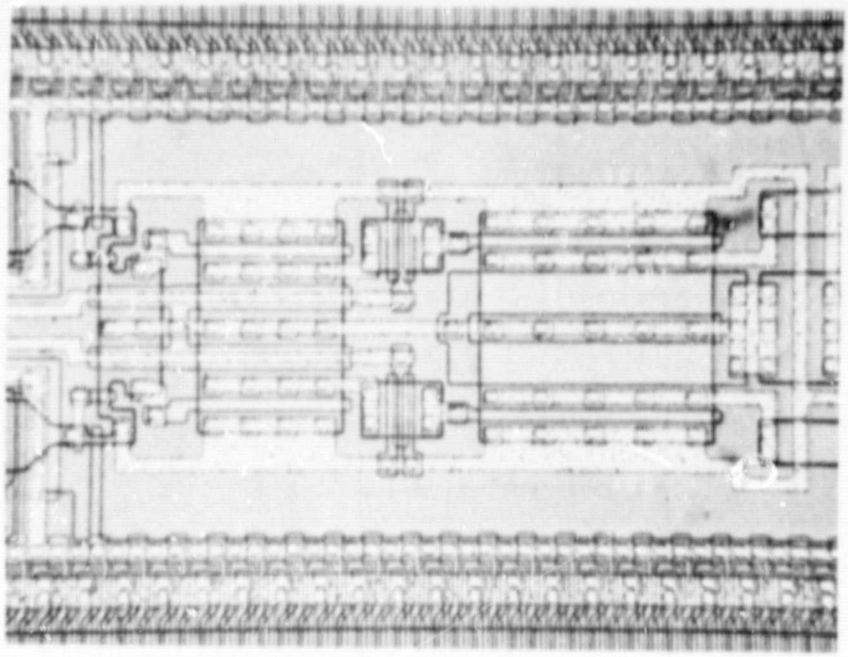


Figure V-13 Output Circuitry, CCD321A; 230X

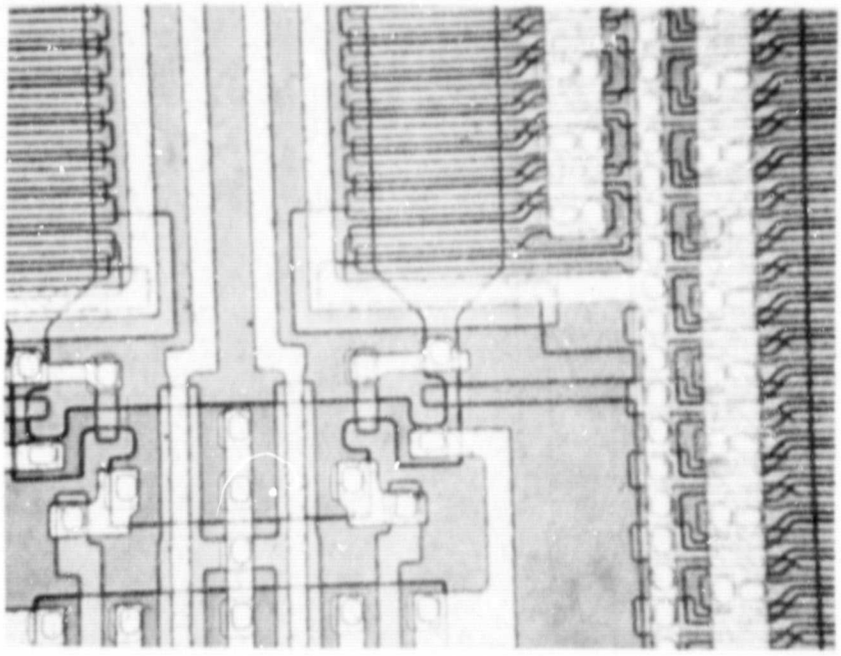


Figure V-14 Interface Between Shift Register and Output, CCD321A; 500X

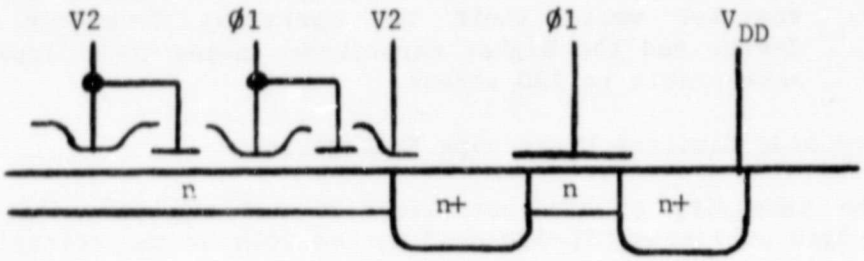


Figure V-15 Output Cross Section, Typical, CCD321A

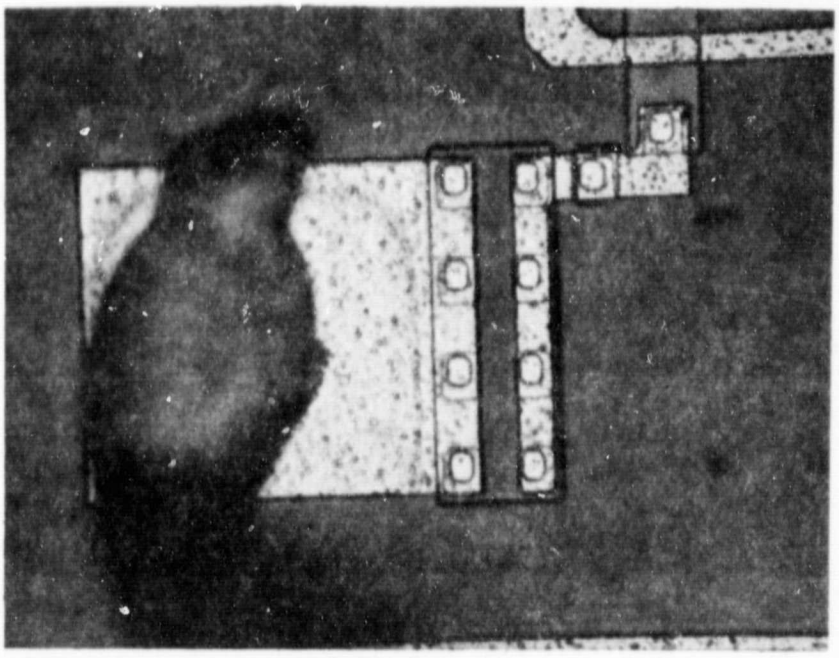


Figure V-16 Input Protect Circuitry, CCD321A; 500X

d. Input Protect Circuit - The inputs which go to a single gate on the chip have an input protect circuit as shown in the photograph in Figure V-16 and in the schematic in Figure V-17. These inputs include V_R, ϕ_S, and ϕ_R. The other gate inputs are protected as shown in the photograph in Figure V-18. These inputs include $\phi 1$ and V_2. The first protect network includes a series polysilicon resistor followed by a diode with the substrate as the anode. The other inputs only have the diode. The probable reason for this is that due to the higher capacitance of the multiple gates a series resistor would limit the operating frequency of the device and the higher capacitance makes these inputs less susceptible to ESD stress.

5. Scanning Electron Microscope Examination

The integrity of the metallization and the polysilicon were judged utilizing MIL-STD-883B Method 2018 as the criteria.

The passivation layer was examined and is shown in Figure V-19. This is the edge of the opening for the bonding pad with the bottom right-hand side being exposed aluminum and the top and left-hand side being covered with passivation. This passivation was seen to be quite thin with portions of the aluminum being exposed along the traces. The passivation covering hillocks along the aluminum traces could not be adequately protected by photoresist and were etched during the bonding window opening etch.

If there are particles present they may bridge between metallization stripes and create shorts at these exposed areas. The other concern is that the aluminum can now be attacked by any corrosive chemical which may be encapsulated within the package. One failure occurred during the life test which may have been partly due to this condition.

Hydrofluoric acid fumes were used to remove the passivation to allow examination of the metallization. A low magnification view of metallization and polysilicon at a corner is shown in Figure V-20. Metallization coverage in a portion of the output amplifier is shown in Figure V-21 and for the contacts to the shift register electrodes in Figure V-22. The electrode contact windows were the worst case step coverage seen on this device. They were acceptable per the specification. A higher magnification view of these are shown in Figures V-23 and V-24. Figure V-23 is the $\phi 1$ contacts to the poly1 on the right and the poly2 on the left. Figure V-24 is the V2 contacts to the poly1 at the bottom and the poly2 at the top. The metallization is approximately 1 micron thick. There is not a reliability risk associated with the coverage on this part. The aluminum metallization was then removed

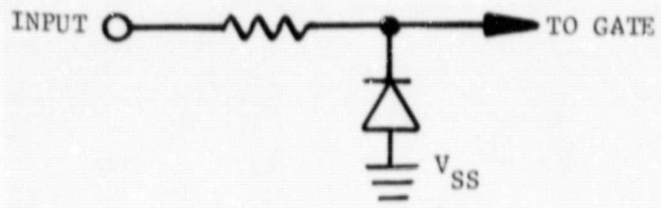


Figure V-17 Schematic, Input Protect Circuit, R5101

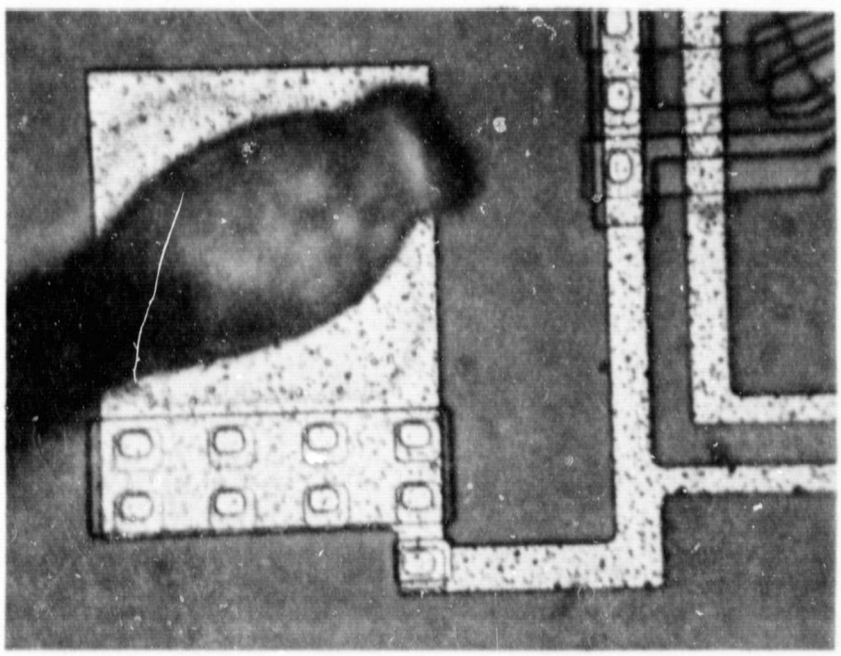


Figure V-18 Input Protect Circuitry, CCD321A; 500X

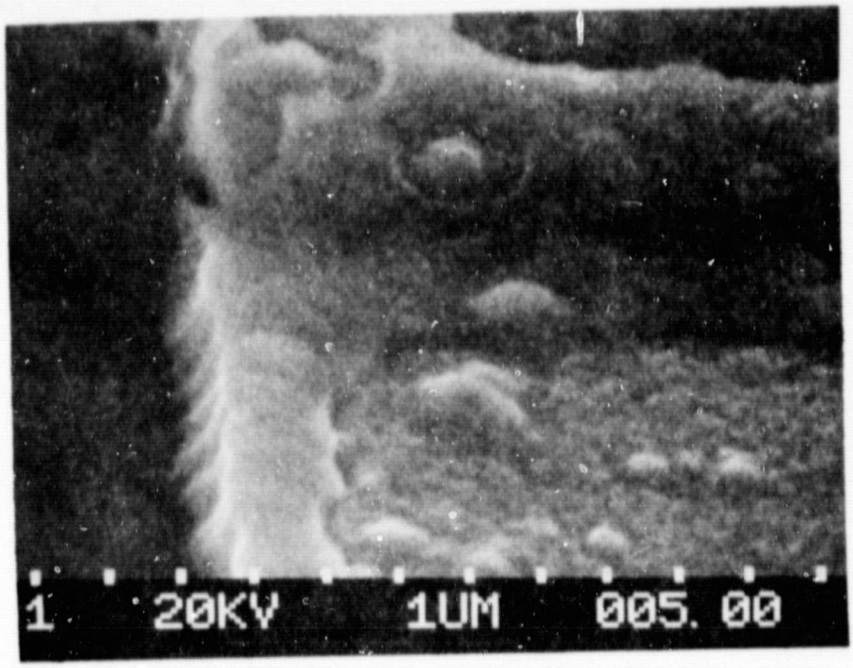


Figure V-19 SEM Micrograph, Passivation Layer, CCD321A; 10000X

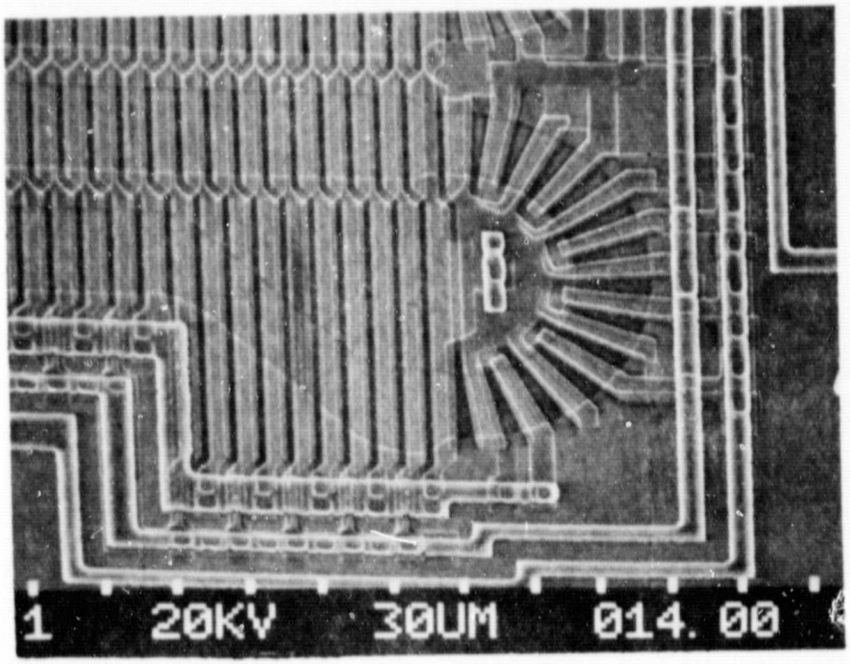


Figure V-20 SEM Micrograph, Corner Structure, CCD321A; 340X

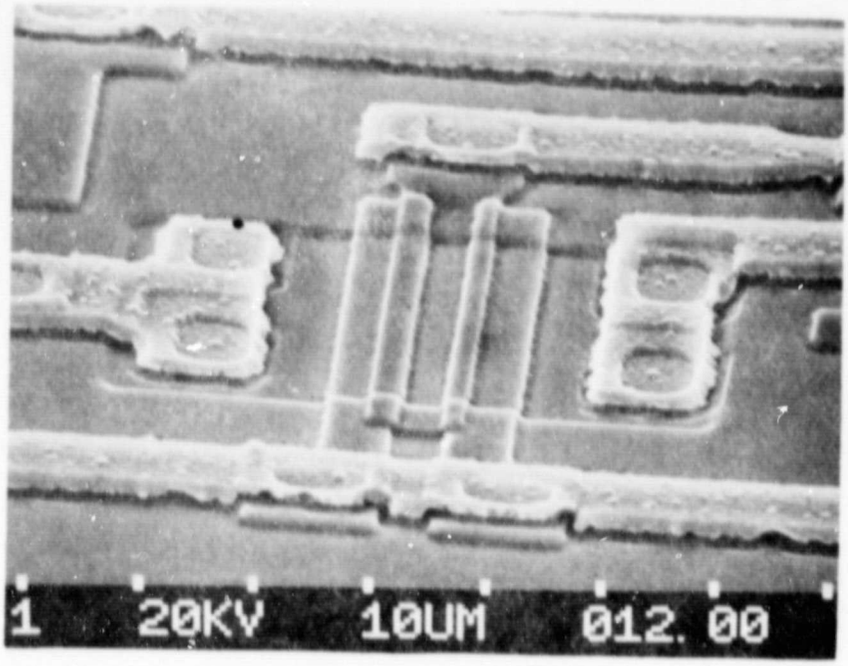


Figure V-21 SEM Micrograph, Metallization Coverage, CCD321A; 1600X

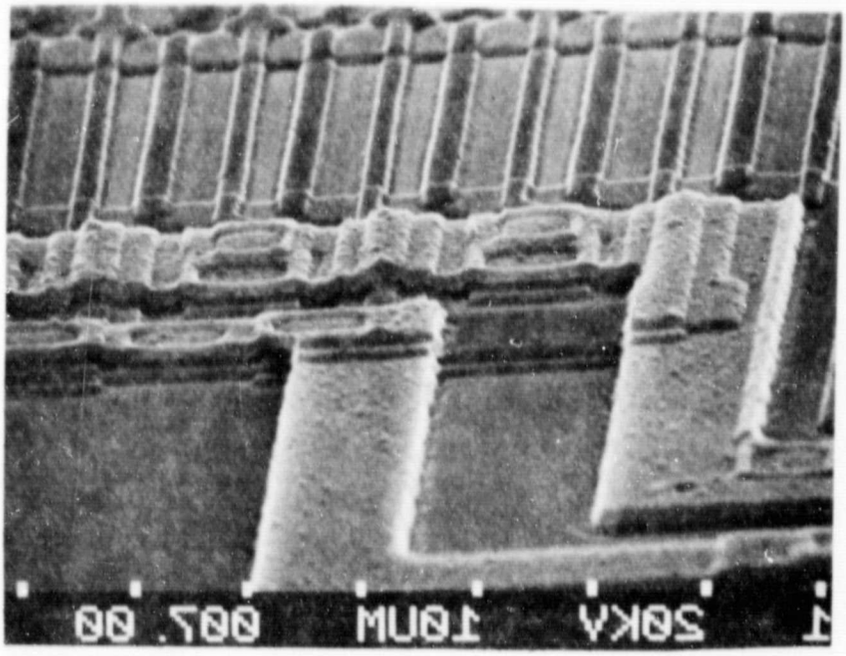


Figure V-22 SEM Micrograph, Metallization Coverage, CCD321A; 1600X

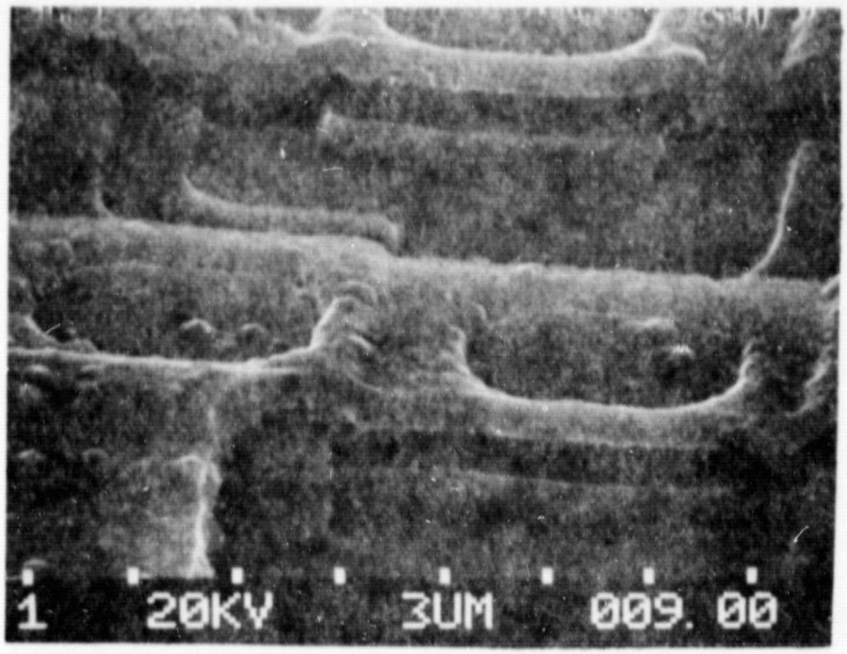


Figure V-23 SEM Micrograph, Metallization Contact Window, CCD321A; 5000X

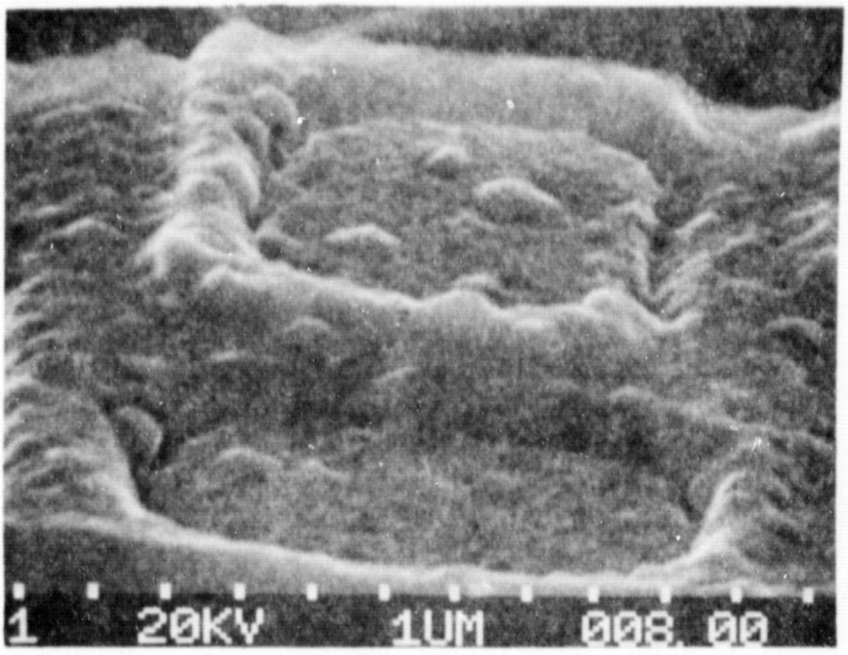


Figure V-24 SEM Micrograph, Metallization Contact Window, CCD321A; 10000X

using Transene Aluminum Etchant. The oxide layer between the aluminum and the polysilicon was seen to be about 6,000 angstroms thick at this time. The area which was shown in Figures V-22 through V-24 was again photographed and is shown in Figure V-25. The oxide layer was then removed using hydrofluoric acid fumes and the polysilicon layers documented.

Figure V-26 shows the output amplifier as well as the surrounding areas. The poly2 layers appear darker in the SEM micrographs. The interface between the shift register and the output amplifier is shown in Figure V-27. This type of examination was used to determine which layer of polysilicon was used for the gates in the amplifier to develop the schematic. An input structure is shown in Figure V-28. A portion of the input protect circuit is visible in the upper left and then the input gates and shift register. Step coverage over thermal oxide steps for poly1 is shown in Figure V-29 and the poly2 coverage is shown in Figure V-30. The poly2 coverage over the poly1 is shown in Figures V-31 and V-32. As is apparent this coverage is excellent. The polysilicon layers are 3,000 to 4,000 angstroms thick and the insulating layer between them appears to be about 1,500 to 2,000 angstroms thick. Two views of the polysilicon at a corner are shown in Figures V-33 and V-34. Figure V-34 shows the surface relief in this area.

The interconnections to the polysiicon gates are shown in Figure V-28. The first gate, ØS, is the lower level polysilicon (poly1). The second gate is VR and then the shift register begins. The first gate in the shift register is a poly1, Ø1 connection. The next two gates are connected to V2. The first gate in this and each pair is a poly2 layer. The next pair is then connected to Ø1. This pattern repeats along the entire shift register.

The SEM examination of the conducting layers found all to be acceptable.

6. Diffusions and Polysilicon Conductors

This section will discuss the diffusions used on this chip and will show these diffusions and the polysilicon conductors in cross-section.

The input protect diode, the input diode, and the output amplifier source and drain diffusions are produced by an n+ diffusion. The shift register diffusion for the channel is produced by a shallow diffusion which is likely formed by ion implantation. An overall view of the chip with the conductor layers stripped is shown in Figure V-35. This shows the input protect diodes, the shift register, and the output amplifier.

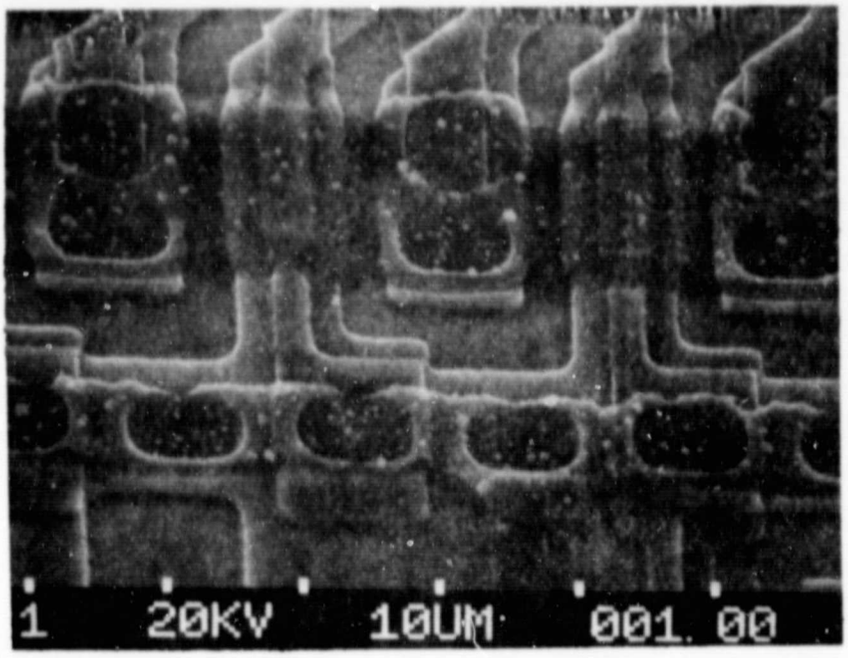


Figure V-25 SEM Micrograph, Oxide Layer, CCD321A; 1900X

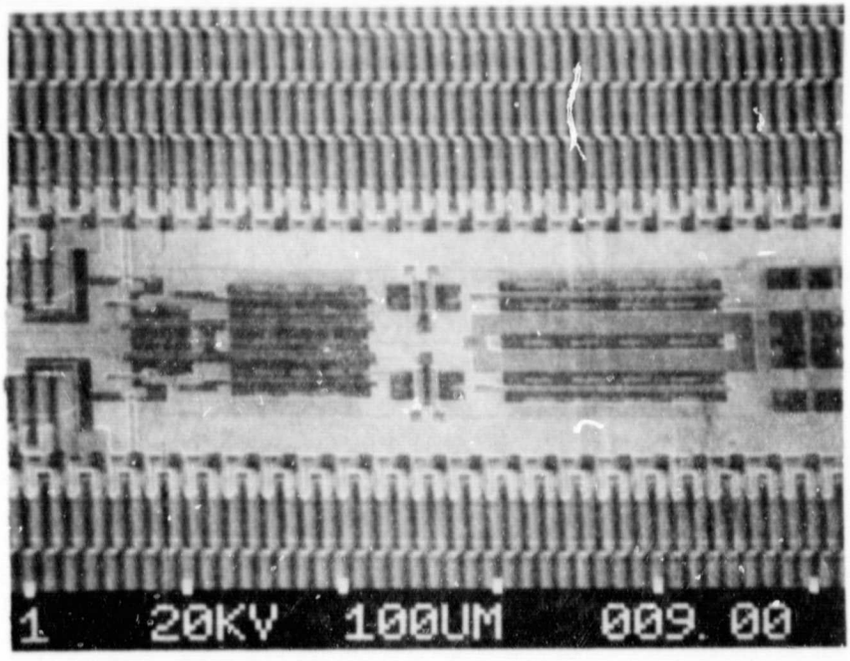


Figure V-26 SEM Micrograph, Output Section, CCD321A; 200X

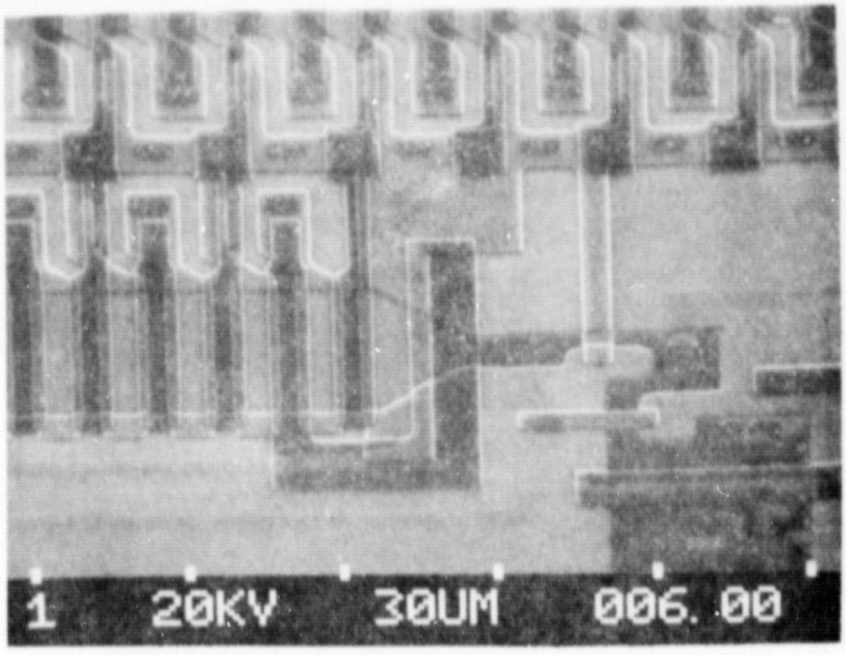


Figure V-27 SEM Micrograph, Polysilicon Coverage, CCD321A; 700X

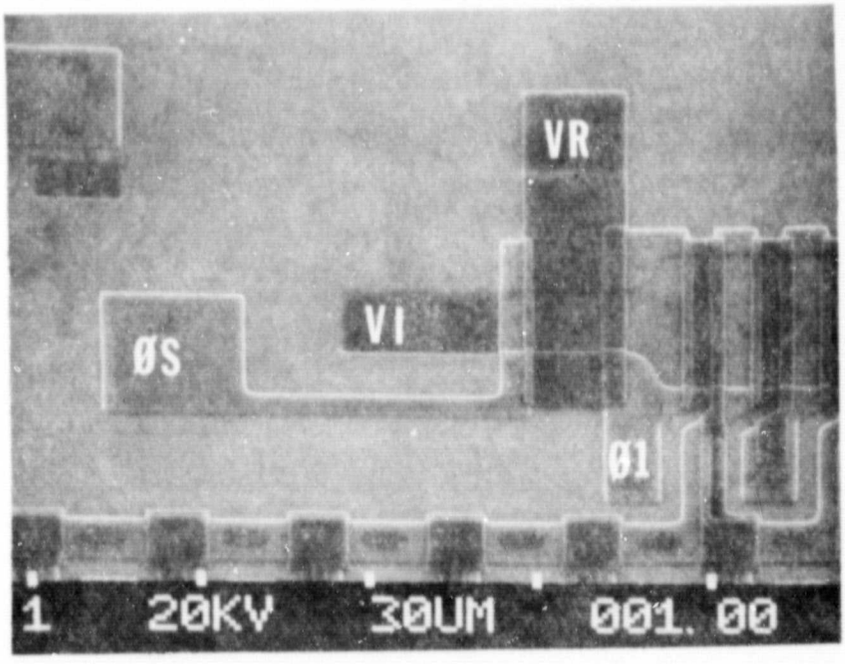


Figure V-28 SEM Micrograph, Input Section Polysilicon, CCD321A; 800X

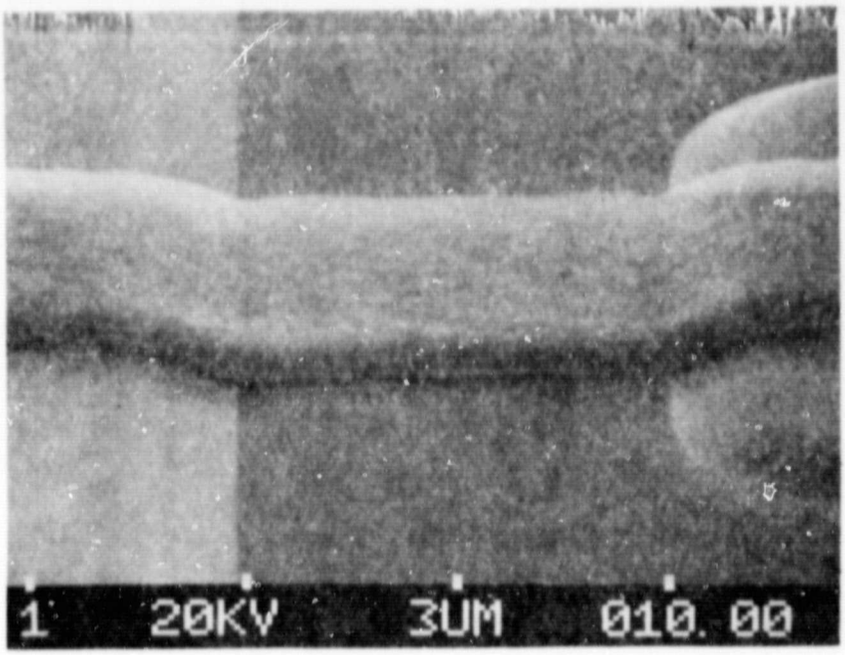


Figure V-29 SEM Micrograph, Poly1 Step Coverage, CCD321A; 10000X

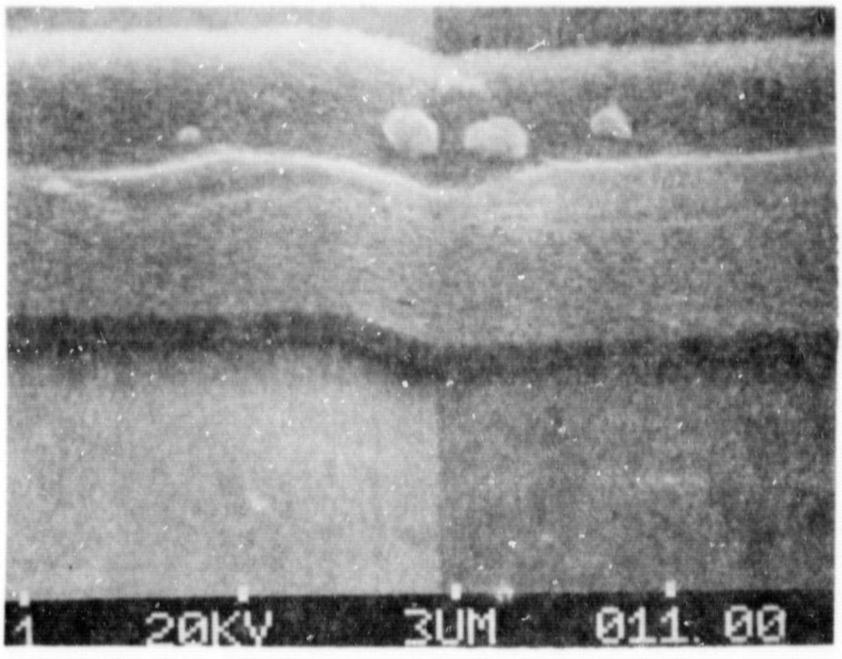


Figure V-30 SEM Micrograph, Poly2 Step Coverage, CCD321A; 10000X

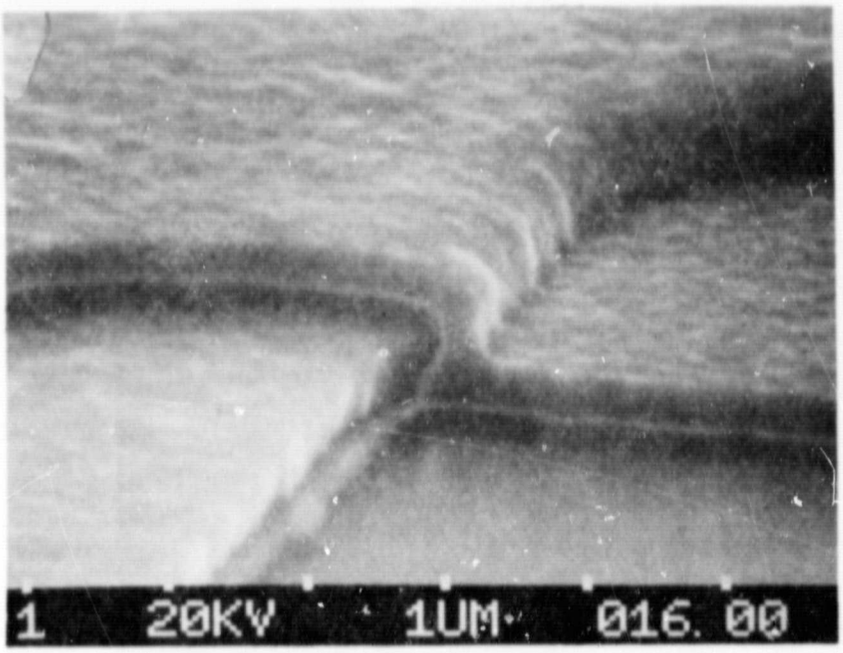


Figure V-31 SEM Micrograph, Poly2 Step Coverage, CCD321A; 19000X

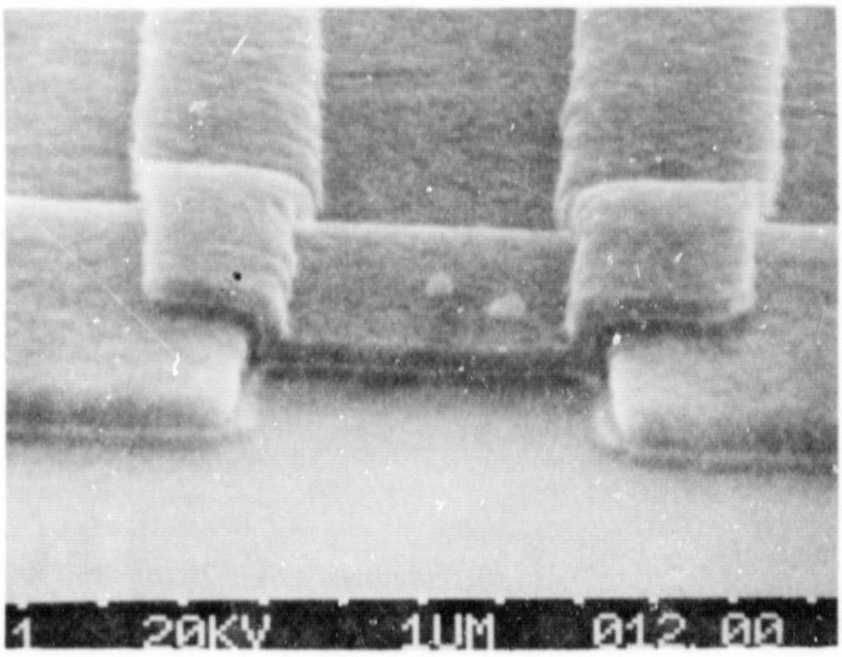


Figure V-32 SEM Micrograph, Output Section Poly2 Step Coverage, CCD321A; 11000X

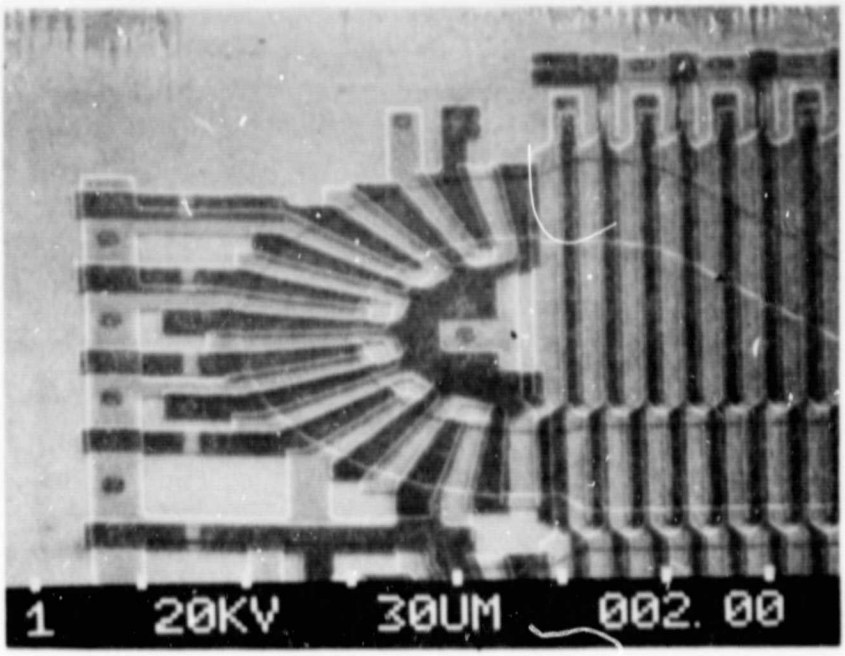


Figure V-33 SEM Micrograph, Polysilicon at Corner, CCD321A; 500X

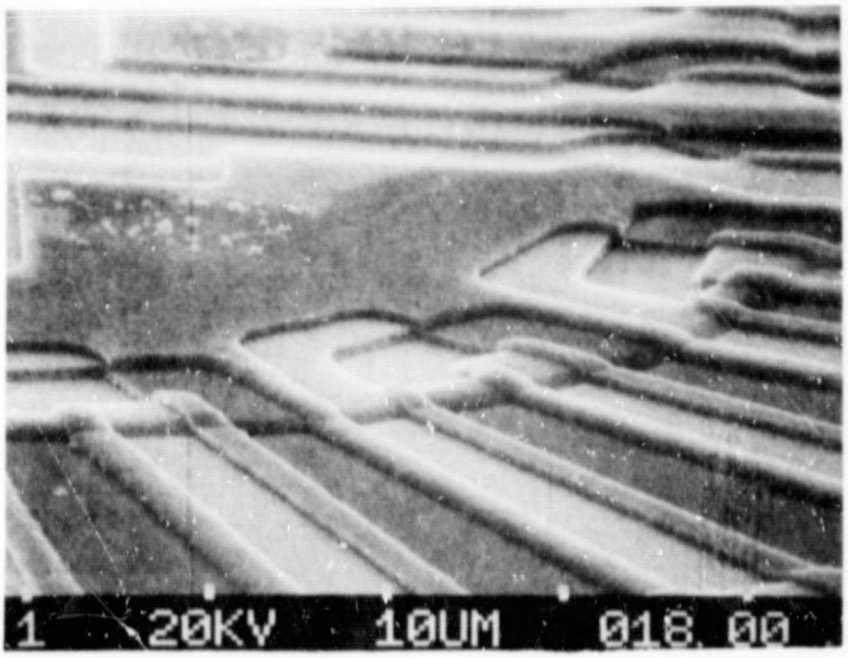


Figure V-34 SEM Micrograph, Polysilicon Step Coverage, CCD321A; 2500X

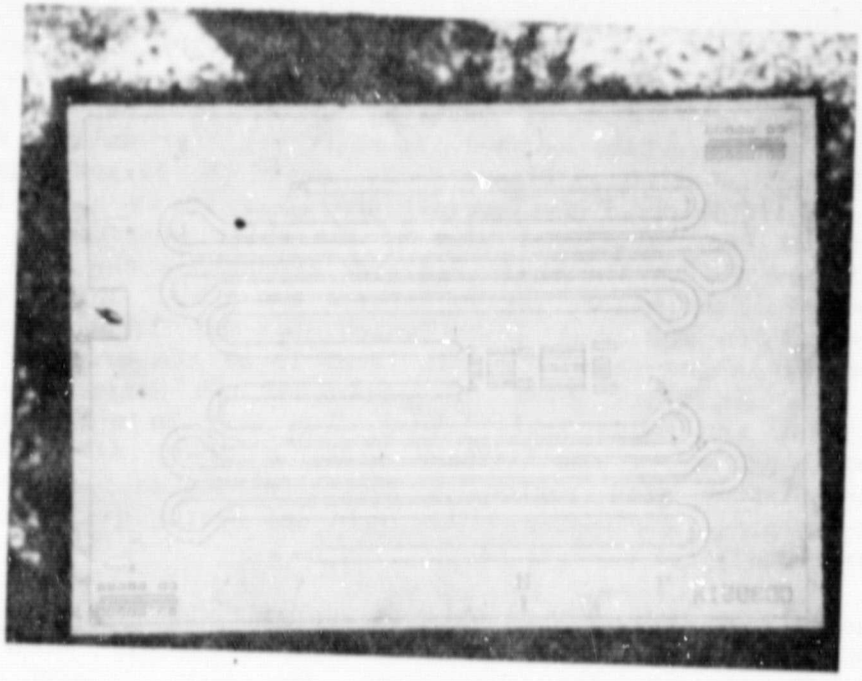


Figure V-35 Die Surface With Diffusions Stained, CCD321A; 40X

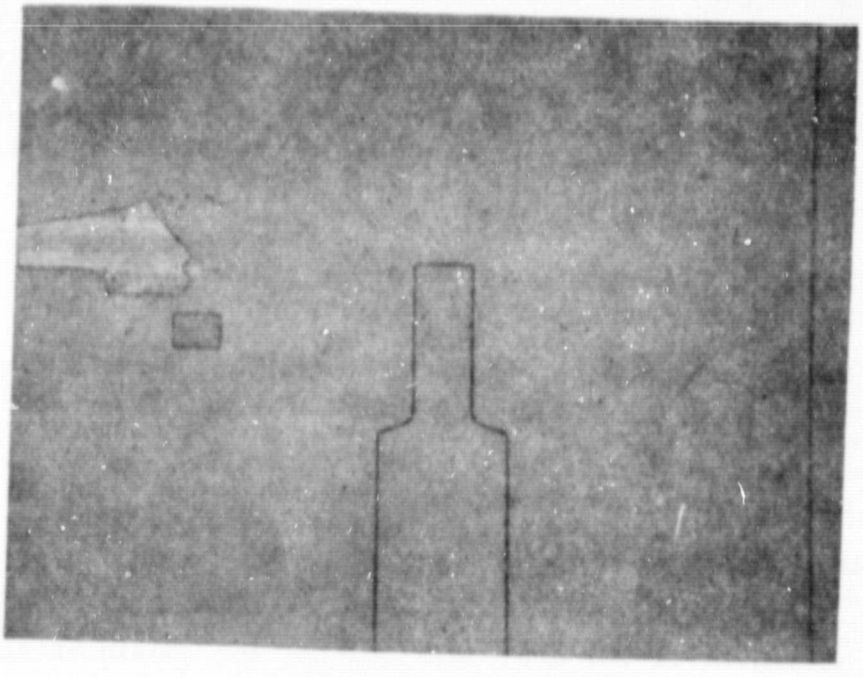


Figure V-36 Input Diffusions, CCD321A; 500X

The input to the shift register and the input protect diode are shown in the photgraph in Figure V-36. The darker area at the start of the shift register is the n+ diffusion. The appearance of the shift register corner is shown in Figure V-37. The interface between the shift register and the output amplifier is shown in Figure V-38. Again the darker areas are the n+ diffusions. The overall amplifier is shown in Figure V-39. A cross-sectional view of the shift register is shown in Figure V-40. The shift register channel is the area which appears as the higher region between two tubs. This area has a thin ion-implanted layer which is the lighter colored material in the channel. This layer is on the order of 2,500 to 3,000 angstroms thick. A portion of the output amplifier is shown in Figure V-41. Going from left to right on this photograph are a non-diffused area, a drain diffusion, an ion-implanted gate region, a source diffusion, and another ion-implated gate region. The drain and source diffusions are approximtely 1.5 microns deep.

Figures V-42 through V-44 show the polysilicon layers. Figure V-42 shows the aluminum metallization above the polysilicon and illustrates the dielectric isolation between these layers. Figure V-43 shows the overlapping polysilicon structure. The right-hand side of the photograph is the shift area region and the left-hand side is the region between channels where the polysilicon is well above the silicon surface. Figure V-44 shows one polysilicon layer crossing over the other layer. This occurs between adjacent shift register channels since the direction of charge flow reverses itself at each corner and therefore the poly1 and poly2 layers that are connected together also have to reverse their order.

B. Electrical Characterization - General

The Fairchild CCD321A data sneet is given in the Appendix. These parts were obtained through a local distributor.

The first group of parts failed due to poor bonds between the gold interconnect wires and the die. Analysis of these bonds indicated too low of a temperature during the thermocompression ball bonding operation. Aluminum ultrasonic bonding was utilized on the second group of parts, which were obtained at no cost from Fairchild.

The second group of parts had 32 out of 50 devices develop leakage current during initial electrical and environmental screen tests. These failures were due to breakdown between the two polysilicon layers. Fairchild is aware of this problem and should be able to solve it.

A third group of parts was obtained at no cost and were used for this study. Failures occurred due to layer-to-layer breakdown, however, not to the extent seen in the second group.

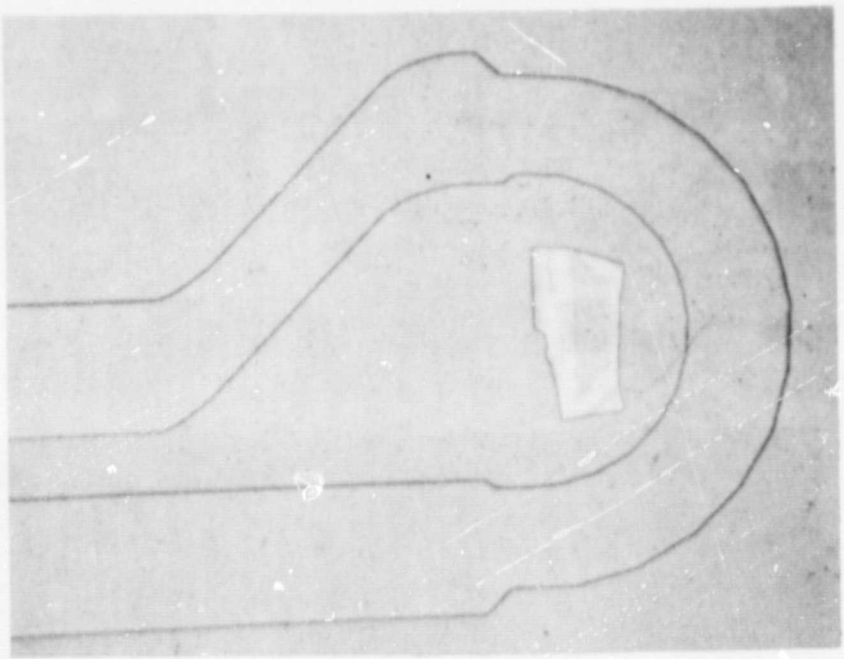


Figure V-37 Diffusion at Corner, CCD321A; 500X

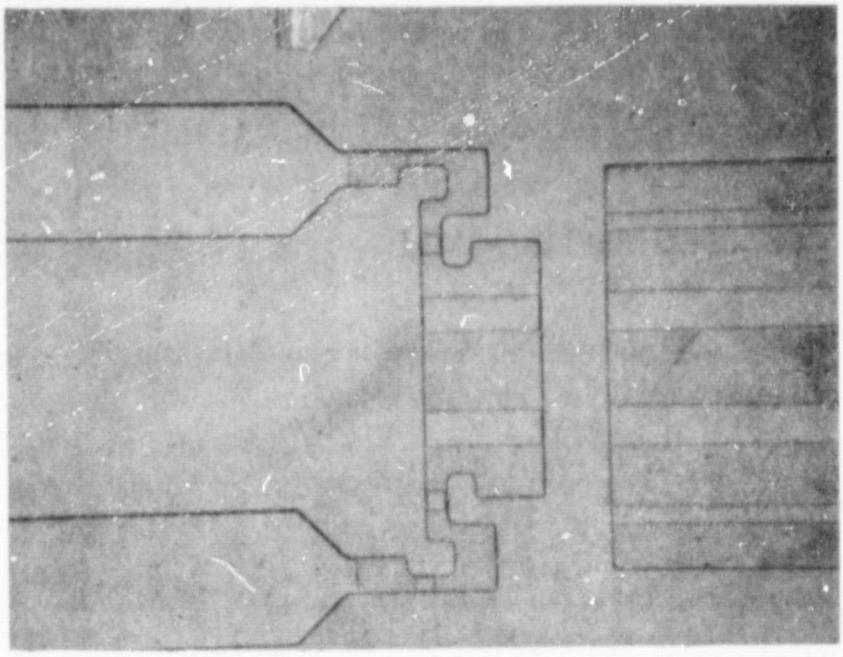


Figure V-38 Shift Register to Output Amplifier Interface Diffusions, CCD321A; 500X

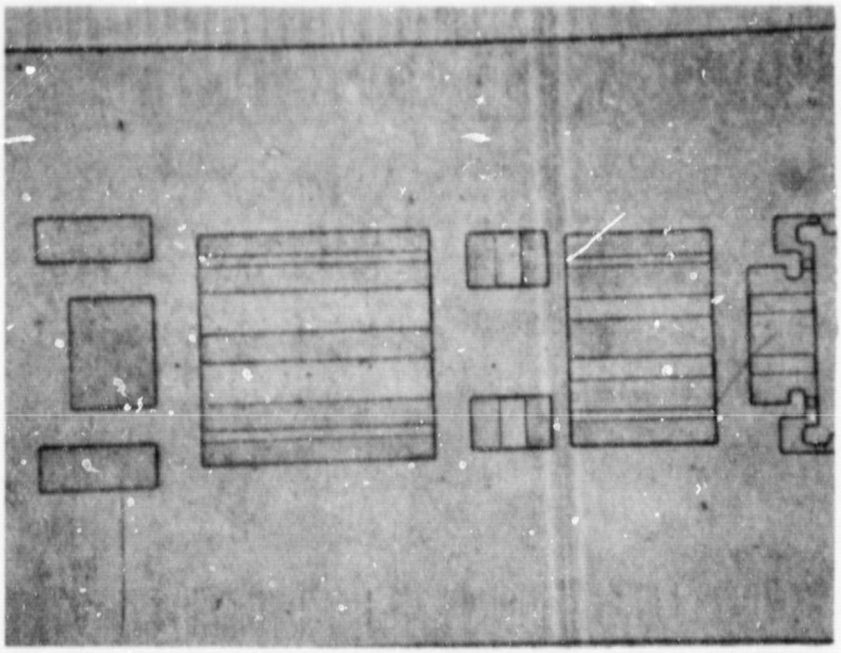


Figure V-39 Output Amplifier Diffusions, CCD321A; 250X

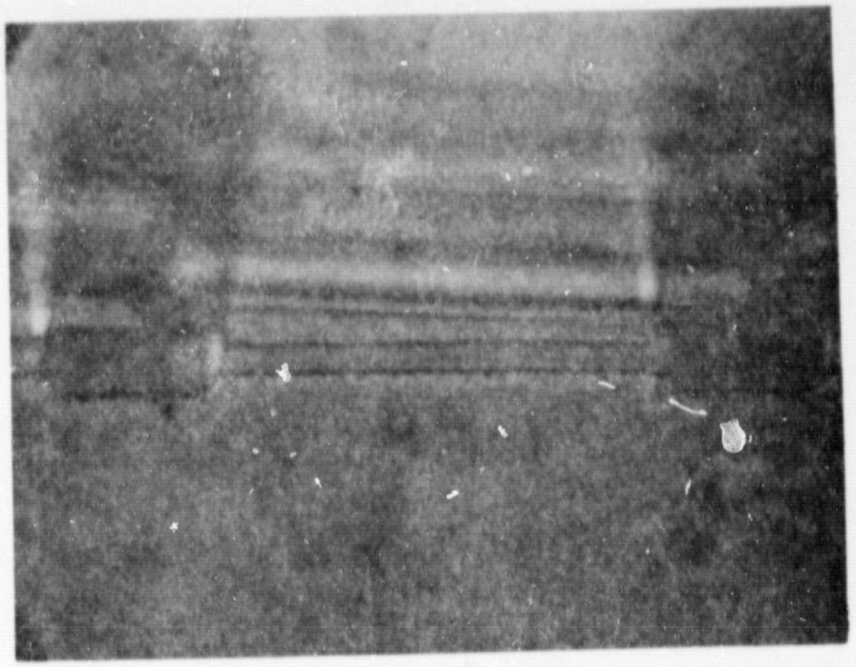


Figure V-40 Cross Section of Shift Register Diffusion, CCD321A; 1000X

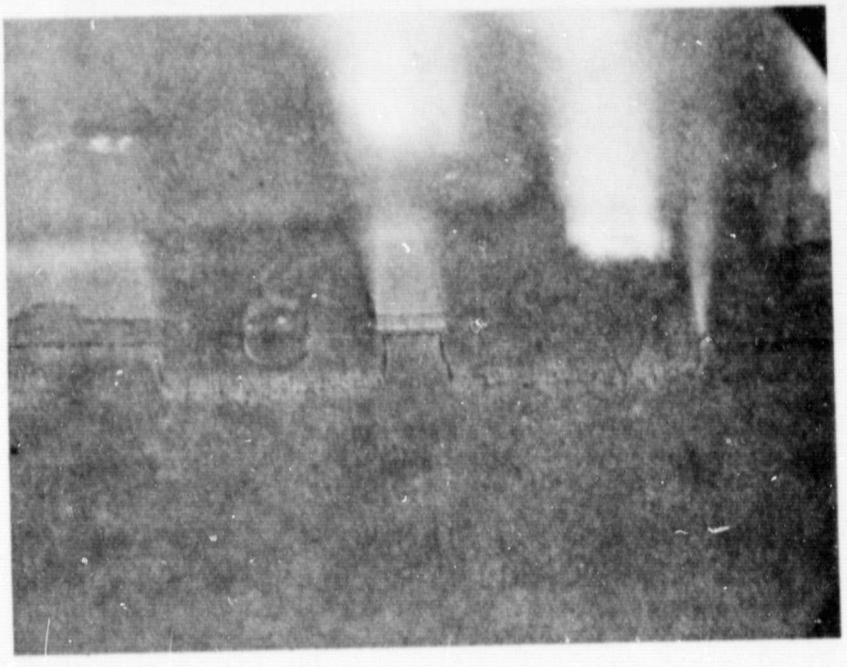


Figure V-41 Cross Section of Output Amplifier Diffusion, CCD321A; 1000X

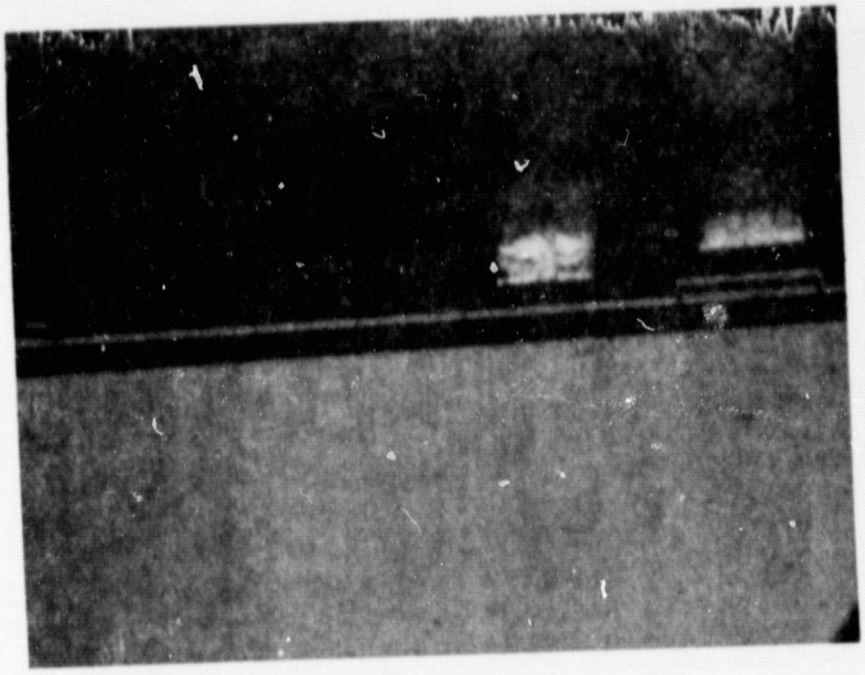


Figure V-42 Cross Section of Polysilicon Layers, CCD321A; 1000X

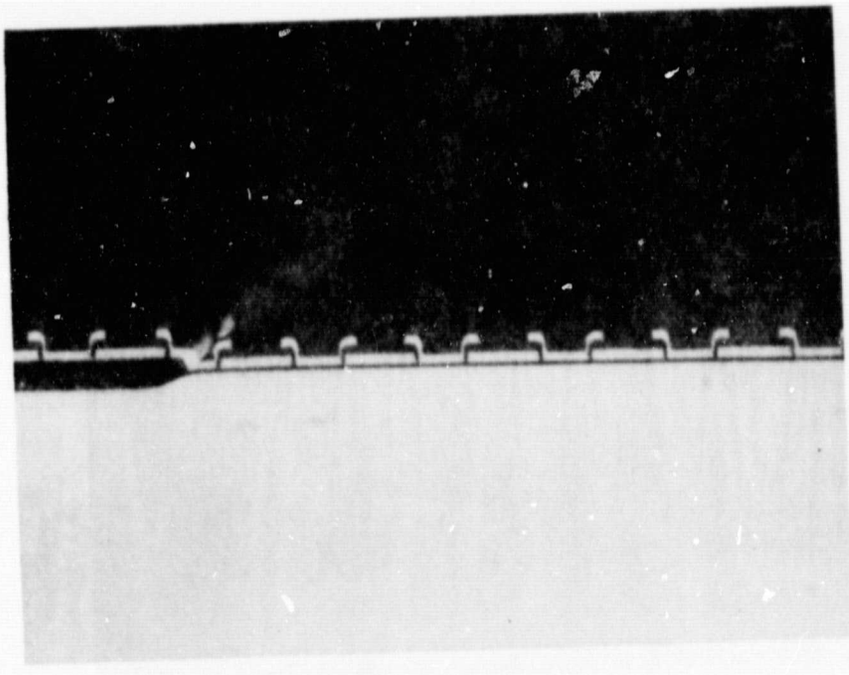


Figure V-43 Cross Section of Polysilicon Layers, CCD321A; 1000X

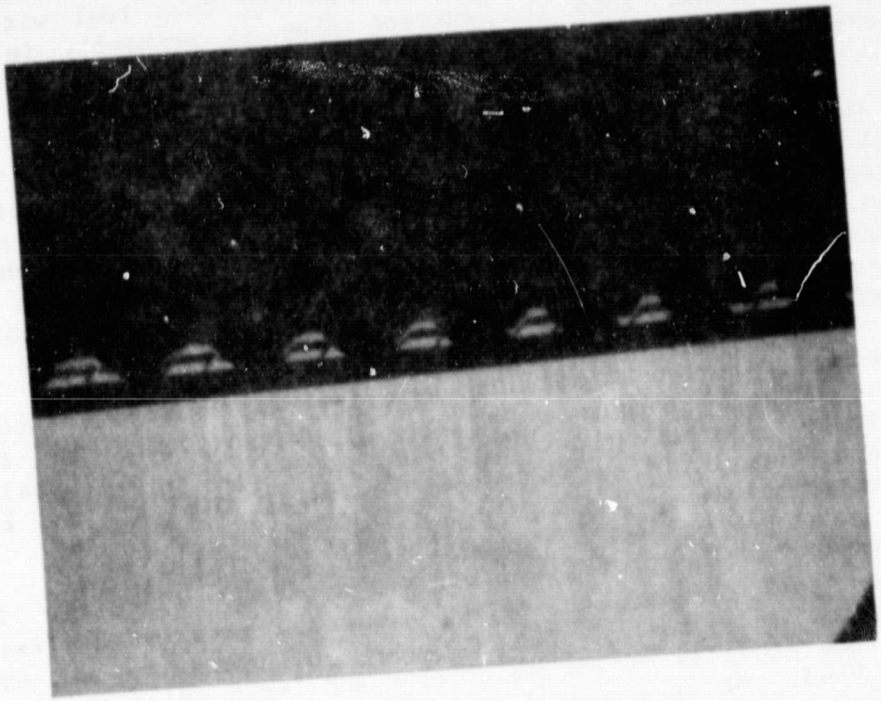


Figure V-44 Cross Section of Polysilicon Layers, CCD321A; 1000X

1. Operating Parameters

Electrical characterization of each of the three groups of parts was performed to determine their operating range. They were operated in the test tool shown in Figure V-45. This tool was designed specifically to operate the CCD321A and perform the electrical tests to be described in this section. The voltages and signals required to operate this circuit are shown in Figure V-45 and in Table V-2.

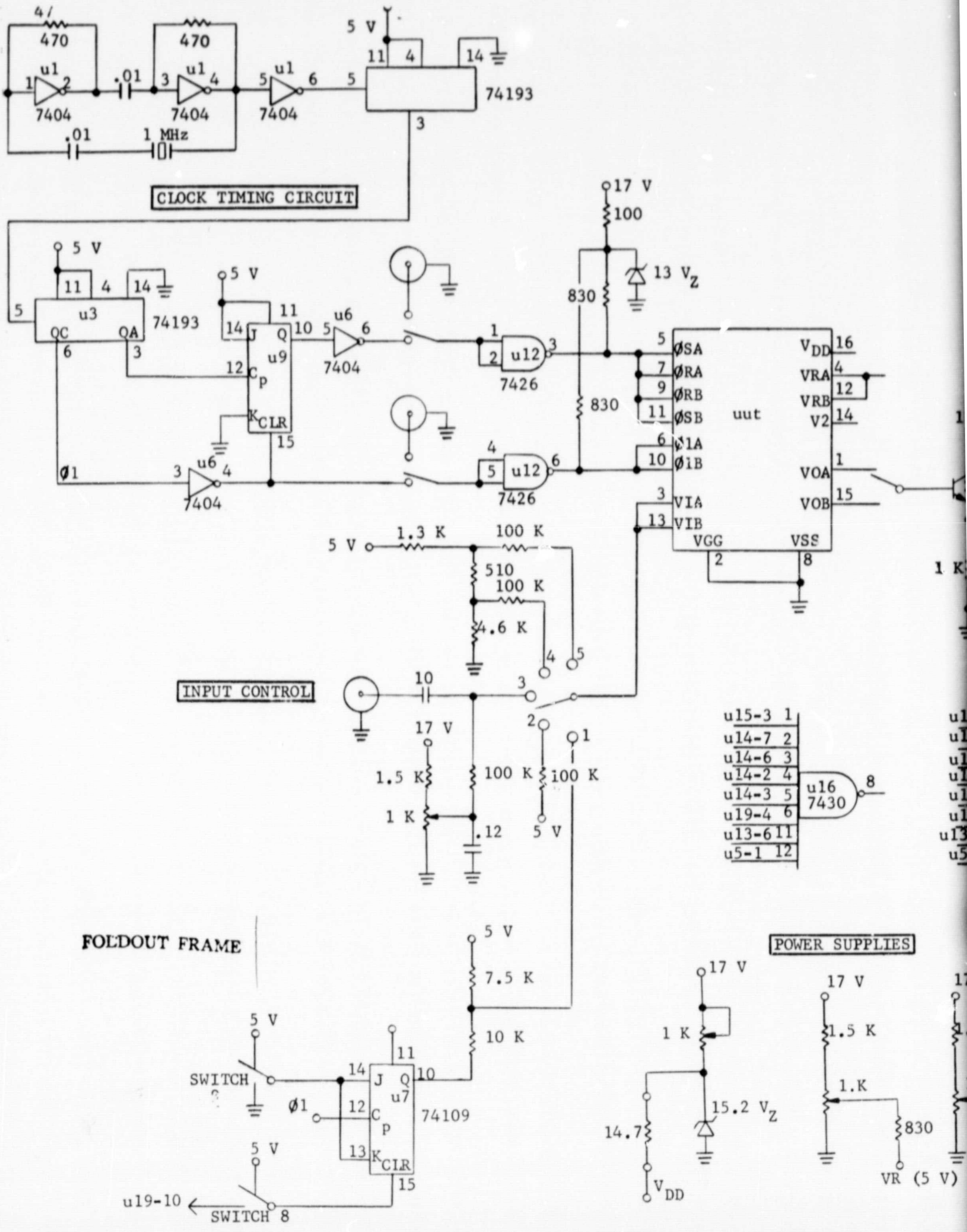
In Table V-2, the first voltage given is the output drain voltage, Pin 16. This voltage is supplied to the output amplifier and to the output load. In the test tool with an emitter follower load the current flow is primarily in the output amplifier. The current level ranged from about 4 to 7 mA.

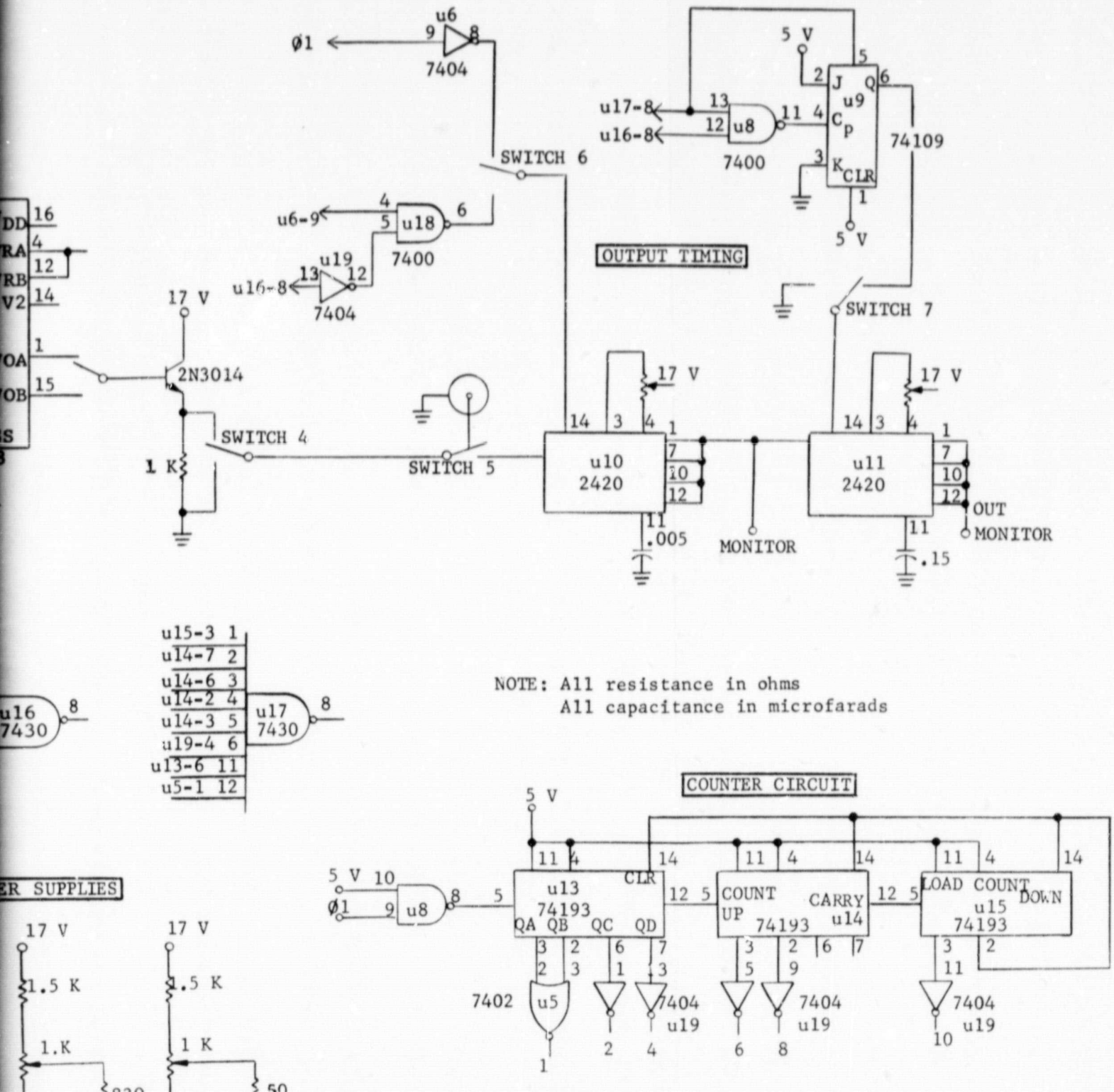
The DC transport voltage is typically given as 6 volts. This level is dependent upon the level of the transport clock voltage and should be approximately one half of its peak value. This level was set at 6.5 volts in the test tool which is one half of the clock voltage level. This voltage is applied to alternate pairs of electrodes along both shift register A and B.

The analog reference inputs can vary from approximately 3 to 7 volts. Signal charge injection is proportional to the difference between the input DC level and this analog reference input. In the test tool VR, going to pins 4 and 12, was set at 5 volts.

The transport clocks, Ø1A and Ø1B are typically 13 volts. In the test tool, an open collector output and gate was utilized to provide this level. The frequency of operation and the timing are provided by the oscillator and logic gates shown in Figure V-45. Ø1 is a square wave at 62.5 KHz. This clock is connected to alternate pairs of gates in the shift register. A full discussion of the transport clock is given in the construction analysis section.

The input sampling clock and the output sample and hold clock are given as typically 13 volts. In the test tool these two clocks are connected together. The timing requirements between Ø1 and ØS are given in the data sheet. In the test tool ØS an ØR go high 2 microseconds after Ø1 goes low and then goes low 2 microseconds before Ø1 returns high. (Figure V-46). The top trace is Ø1 and the bottom trace is ØS. These traces are at 10 volts per vertical division and 5 microseconds per horizontal division.


CLOCK TIMING CIRCUIT
INPUT CONTROL
FOLDOUT FRAME
POWER SUPPLIES
74193
7404
7426
74109
7430
uut
1 MHz
SWITCH 8
u19-10
VR (5 V)



FOLDOUT FRAME 2

Figure V-45 Schematic, Test Tool, CCD321A

TABLE V-2 OPERATING VOLTAGES, CCD321A

VOLTAGE FUNCTION	SYMBOL	RANGE		
		MIN	TYP	MAX
OUTPUT DRAIN	V_{DD}	14.5	15.0	15.5
DC TRANSPORT PHASE	V2		6.0	
ANALOG REFERENCE INPUTS	VRA, VRB		3-7	
TRANSPORT CLOCK	Ø1A, Ø1B	12.0	13.0	15.0
INPUT SAMPLING CLOCK	ØSA, ØSB	12.0	13.0	15.0
OUTPUT SAMPLE & HOLD CLOCK	ØRA, ØRB	12.0	13.0	15.0
INPUT DC LEVEL	VIA, VIB		3-7	

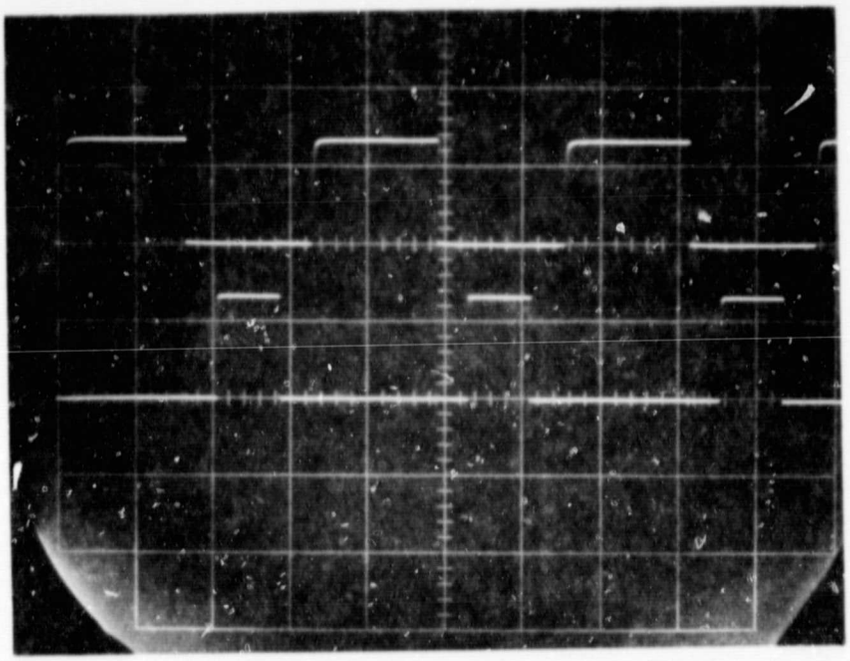


Figure V-46 Ø1 and ØS Clock Pulses, CCD321A

The input DC level can range from 3 to 7 volts typically. There are five positions which can be connected to the input on the test tool. The function of each of these will be discussed in the appropriate electrical measurement section. For initial characterization, position 3 was used and the transfer characteristic was developed. Figure V-47 shows the transfer characteristic for one device from the first lot, Date Code 7901, and from the third lot, Date Code 7952. Two curves are shown for the same device from the D.C. 7952 lot with VR at 5.0 volts and 6.0 volts. There was some variation of this transfer characteristic within each lot. This is a function of many manufacturing parameters.

The signal outputs on this device are pins 1 and 15. The emitter follower output provides the output voltage levels as given in figure V-47. The output level is valid when ØR is low. When ØR is high the charge on the output gate is reset and the voltage present at that time is not related to the analog level from the shift register. To avoid any transient problems on the test tool the sample times on the sample and hold circuits occurs when Ø1 is high. This is within the valid portion of the output voltage.

Two pins on this device, V_{GG} and V_{SS} were connected to ground. These are pins 2 and 8 respectively.

Table V-3 lists the electrical measurement made on the CCD321A-2 devices. The temperatures utilized for this testing were +25^{O}C, -25^{O}C, and +55^{O}C. The high and low temperatures used are the maximum ratings specified for this part. The initial electrical characterization was utilized to provide in-depth information about the performance of these devices. The objective of the post environmental characterization tests was to determine delta shift information on each device. The interim electrical tests assured that the devices were funtional at the specified points in the test and also were used to obtain additional parametric data for delta shift analysis.

2. Electrical Parametric Measurements

   a. Device Power - This is a measure of I_{DD} which comprises essentially all of the input current to the CCD. This measurement provides information about the stability of the output amplifier. There are three stages for the amplifiers on each side of the device and each stage is internally loaded with current "pull down" loads. Depending upon geometry and drain and source diffusions, the transistor channel resistance will vary somewhat between devices. This will cause a difference in the current measured for different parts. A change in this current can be indicative of threshold voltage drift,

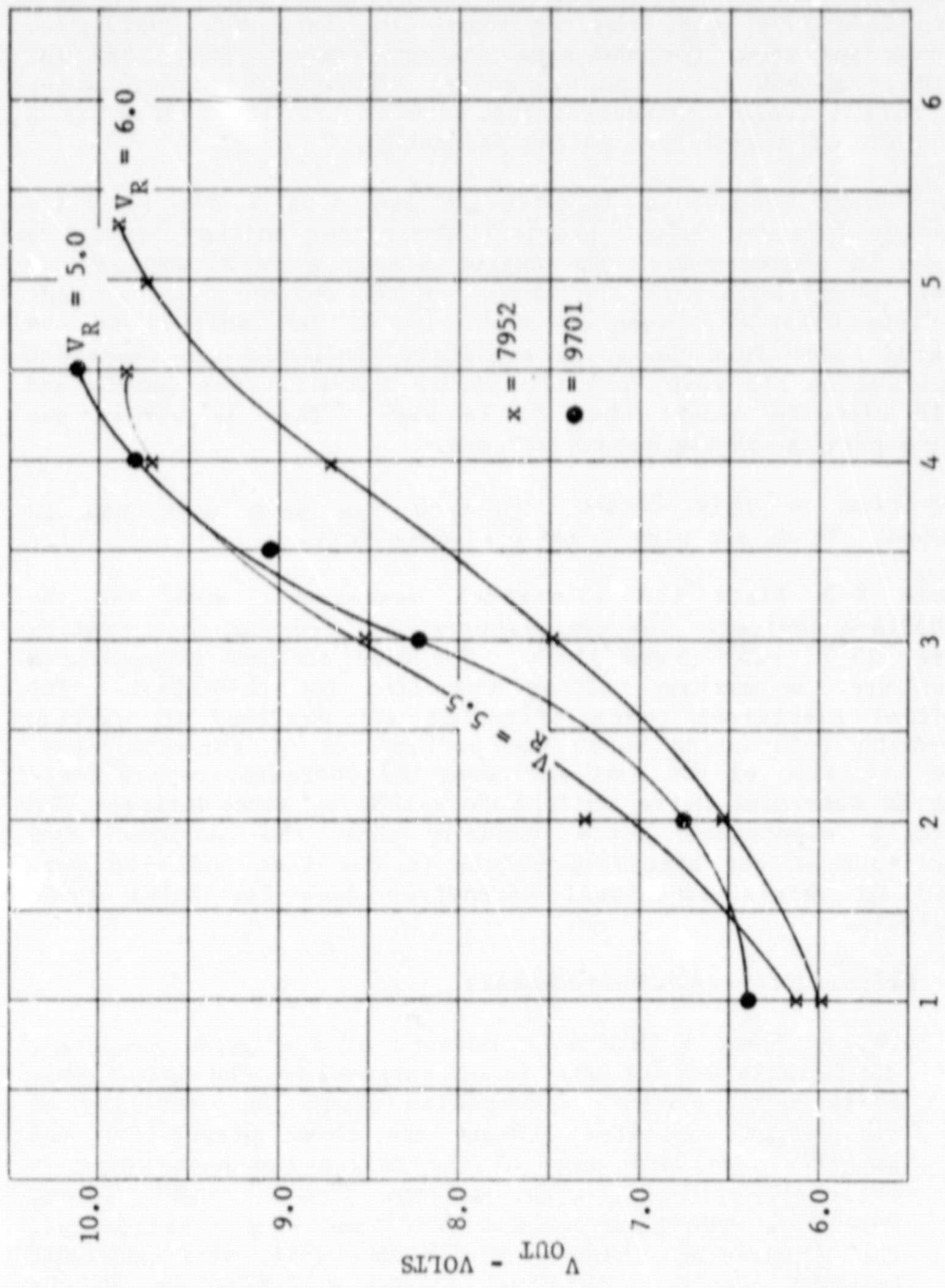


Figure V-47 Transfer Characteristics, CCD321A

TABLE V-3 ELECTRICAL TESTS, CCD321A

SEQUENCE	TEMPERATURE	TEST TYPE
1) INITIAL CHARACTERIZATION	25, -25 & 55°C	FULL
2) POST ENVIRONMENTAL SCREEN	25°C	INTERIM
3) POST 160 HR BURN-IN	25°C -25 & 55°C	FULL INTERIM
4) STEP STRESS	25°C	INTERIM
5) HIGH TEMP LIFE TEST @ 4, 8, 16, 32, 64, 128, 256, 500, 1000 & 2000 HOURS	25°C	INTERIM
6) POST HIGH TEMP LIFE TEST	25°C	FULL
7) TEMPERATURE CYCLING @ 20, 50, 250, 500 & 1000 CYCLES	25°C	INTERIM

NOTE: Interim electricals = Output Drain Current, Gain, Offset Voltage and Input Leakage Currents.
Full electricals = Interim Electricals plus - Noise, Transfer Efficiency and Bandwidth.

shorting (or leakage current paths) between the two polysilicon layers, between the polysilicon and metallization, or between the polysilicon gates down to the silicon. This current was measured on the test tool by reading the voltage drop across a 14.7 ohm resistor and calculating the current flow. A typical value for this reading was 0.0882 volts which calculates out as 6 mA.

b. Input Gate Leakage - Input gate leakage is measured on the leakage current test tool shown in Figure V-48. The inputs measured were Ø1A, ØSA, VRA, ØRA, V2 ØRB, ØSB, VRB, and Ø1B. A constant 11 volts is applied to each of these inputs through a 100 kohm limiting resistor. The voltage is then measured across each of these resistors and recorded. Resolution down to .0001 volts was utilized which provided a current sensitivity of 1 nanoamp. This measurement is important to CCDs since one of the most prominent failure modes is leakage current between overlapping polysilicon layers. The above measurement will detect this type of layer to layer short if one of the layers is connected back to V_{DD}, V_{GG}, or V_{SS}. From the information gained through the construction analysis and failure analysis portions of this study, additional leakage paths should be measured. These include any pin combinations which are connected to adjacent polysilicon gates that overlap. For the CCD321A-2 this includes: ØSA to VRA, VRA to Ø1A, Ø1A to V2, ØSB to VRB, VRB to Ø1B and Ø1B to V2. The failure analysis section will discuss electrical parametric shifts which resulted from leakage paths between some of the above combinations.

c. Voltage Offset - This term describes the buried channel "dark current". This current is produced by thermally generated minority charge in the bulk silicon (electrons in the N doped buried channel which is depleted by channel bias). This is a temperature sensitive measurement since the dark current doubles for every 8 to 10^{O}C.

In the test tool this measurement was made by setting the input to position 2, 5 volts, and reading the output voltage level. The output voltage read is the level produced with no charge input to the shift register.

The output amplifier schematic was shown in Figure V-12. With the clock circuits as indicated previously this output circuit functions in a sample and hold mode. ØR goes high and applies a charge level to the output transistor. The output voltage level with ØR high is related to the feedthrough of this signal and not to an

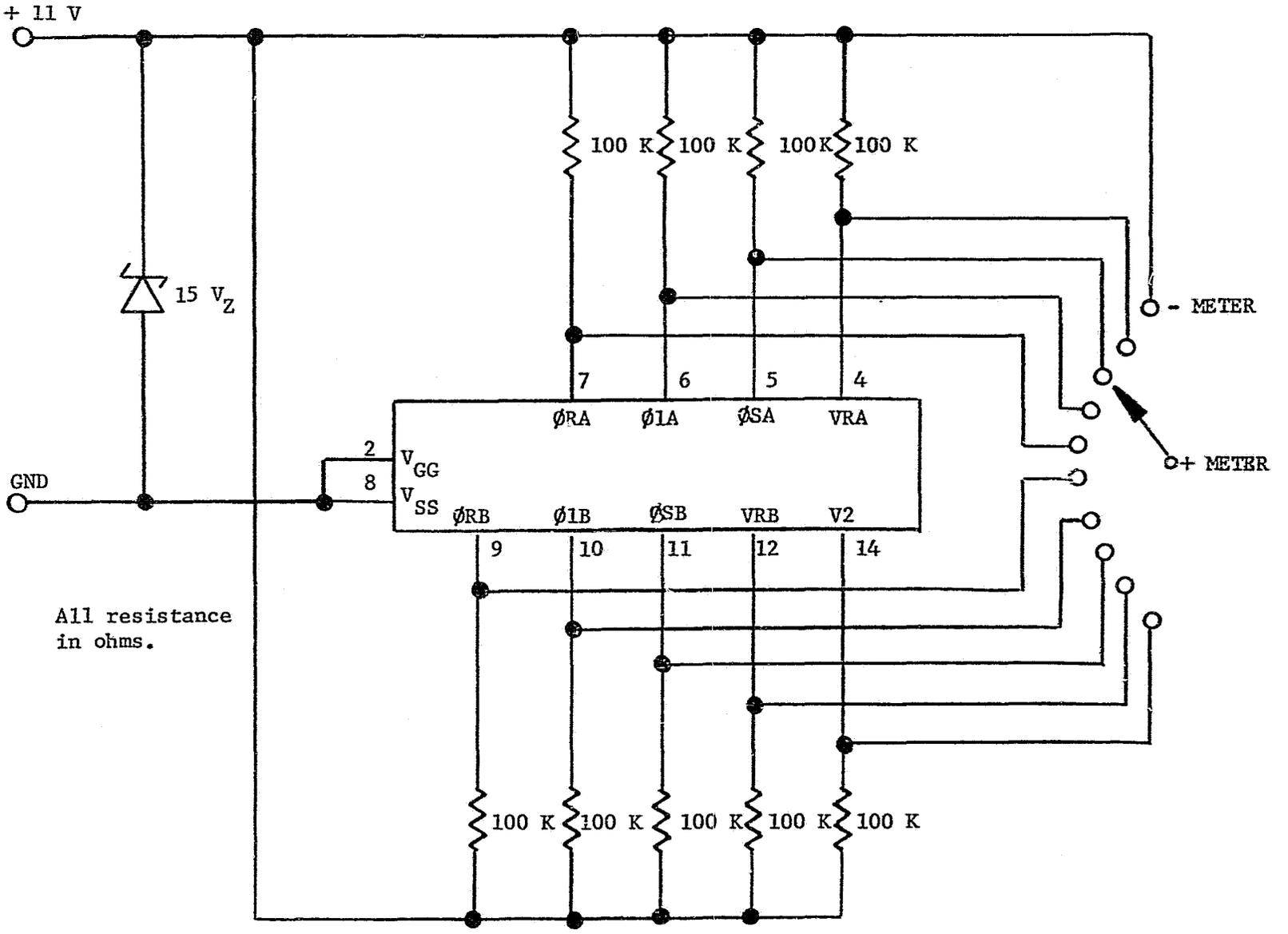


Figure V-48 Schematic, Leakage Test Tool, CCD321A

offset voltage level. It is not possible in this configuration to measure the reset level and then subtract the analog output level from it in order to measure an offset value that is independent of the output amplifier characteristics. If ØR was held at V_{DD}, the output signal would then be a square wave with half of its duration equal to the output reset level and the other half related to the charge from the shift register. This would allow a measurement to be made which would remove any output amplifier variation from the value read.

The readings taken on a typical device for Voffset are: -25°C = 9.93V, +25°C = 10.11V, +55°C = 9.99V. These readings indicate that two conditions on the chip are changing and they are changing with opposite temperature coefficients. The dark current level will increase with temperature which will cause the output level to decrease. This appears to be the significant factor for the decrease above 25°C. Below 25°C the output level also decreases. This is apparently due to a change in the amplifier characteristic with temperature. Temperature characterization of this phenomena found the peak output level to be at about 25°C.

d. Voltage Gain - The voltage gain is performed by measuring the output voltage level change for a known change in the input voltage level. In the test tool, readings were taken with the input switched to position 5 (3.9V) and then with the input switched to position 4 (3.5V). The second output level subtracted from the first, divided by 0.4 volts is equal to the gain. A change in the gain would indicate a change in the input sensitivity, the transfer efficiency, or the output amplifier gain. The input levels were selected by utilizing the characterization data shown in Figure V-47.

e. Noise Measurement - CCD noise is partially a function of the magnitude of the dark current since random noise can be produced due to the shot noise of the electronic charge. It is also affected by input circuit charging noise, reset circuit charging noise, output amplifier noise, and surface and bulk state trapping noise along the shift register. To take the noise measurement on the test tool the input was set to position 5, switch 6 was set to U18-6, and switch 7 was set to U9-6. The first sample and hold circuit acquires the output level at a valid portion of this signal. The signal is sampled at the time when U18-6 goes low with a sample time of 8 microseconds. The 5000 pF holding capacitor provides accuracy to 0.1% in 6 microseconds on U10. The second sample and hold, U11, is held in the sample position

starting at the same time as U10 and remaining for 720 microseconds. With the 0.15 microfarad capacitor this circuit will reach 0.1% accuracy in 700 microseconds. These two sample and hold circuits in series provide the necessary fast sampling time as well as the slow output level drift to read individual voltage levels on the output. In this circuit configuration a new sample is read every 8 milliseconds while the computer accepts a sample every 250 milliseconds. To obtain an RMS voltage reading, 125 samples are accepted and this value calculated.

$$(\text{RMS Noise})^2 = \sum_{i=1}^{125} (X_i - \bar{X})^2$$

There were two problems associated with taking this measurement. The first one was the system noise since there were several A.C. signals in the test tool. This could result in erroneous readings being taken by the computer. The second problem was the change in the output voltage level as the chip heated up while operating. The output voltage drift with time as the chip is heating up is shown in Figure V-49. With this device in the test tool for 140 seconds the output level went from 9.3750 to 9.4250. This is a change of 50 mV. Since the amount of change decreases with time the output noise level for the first side read will be higher than the second side. This was evident during the electrical testing on these devices. Side B was measured first and was consistently higher.

f. Bandwidth - A separate test tool was constructed for the bandwidth measurement (Figure V-50). The other test tool had the necessary interconnections to perform a bandwidth test, however, due to the amount of wiring very poor wave shaping resulted on the two clock signals. On the bandwidth test tool both sides A and B are shown connected at one time, however, during the actual testing only one side was connected to the clock signals. All of the devices were tested on Side A and then the wires were soldered to side B and it was tested. This provided better clock pulse waveshape. Two separate 9644 drivers, which were obtained at no cost from Fairchild, were used as the drivers. These circuits produced a 0 to 13 volt square wave output of opposite polarity to the input. The input timing was produced by an HP 8016b Word Generator for Ø1 and by an HP 1900 Pulse Generator for ØR and ØS. The Pulse Generator was driven by the Word Generator. The analog signal input was supplied by a

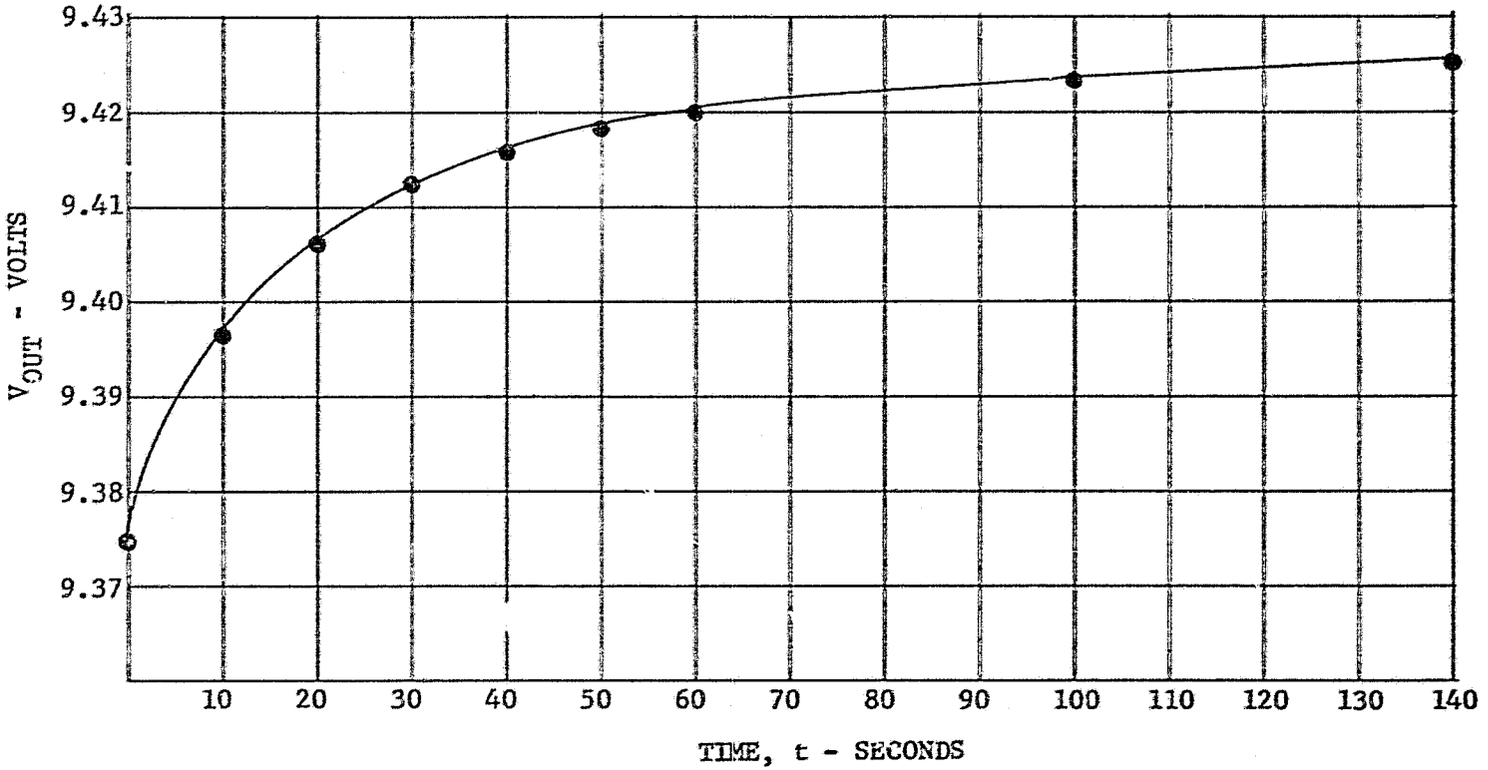


Figure V-49 Voltage Out vs Warm-up Time, CCD321A

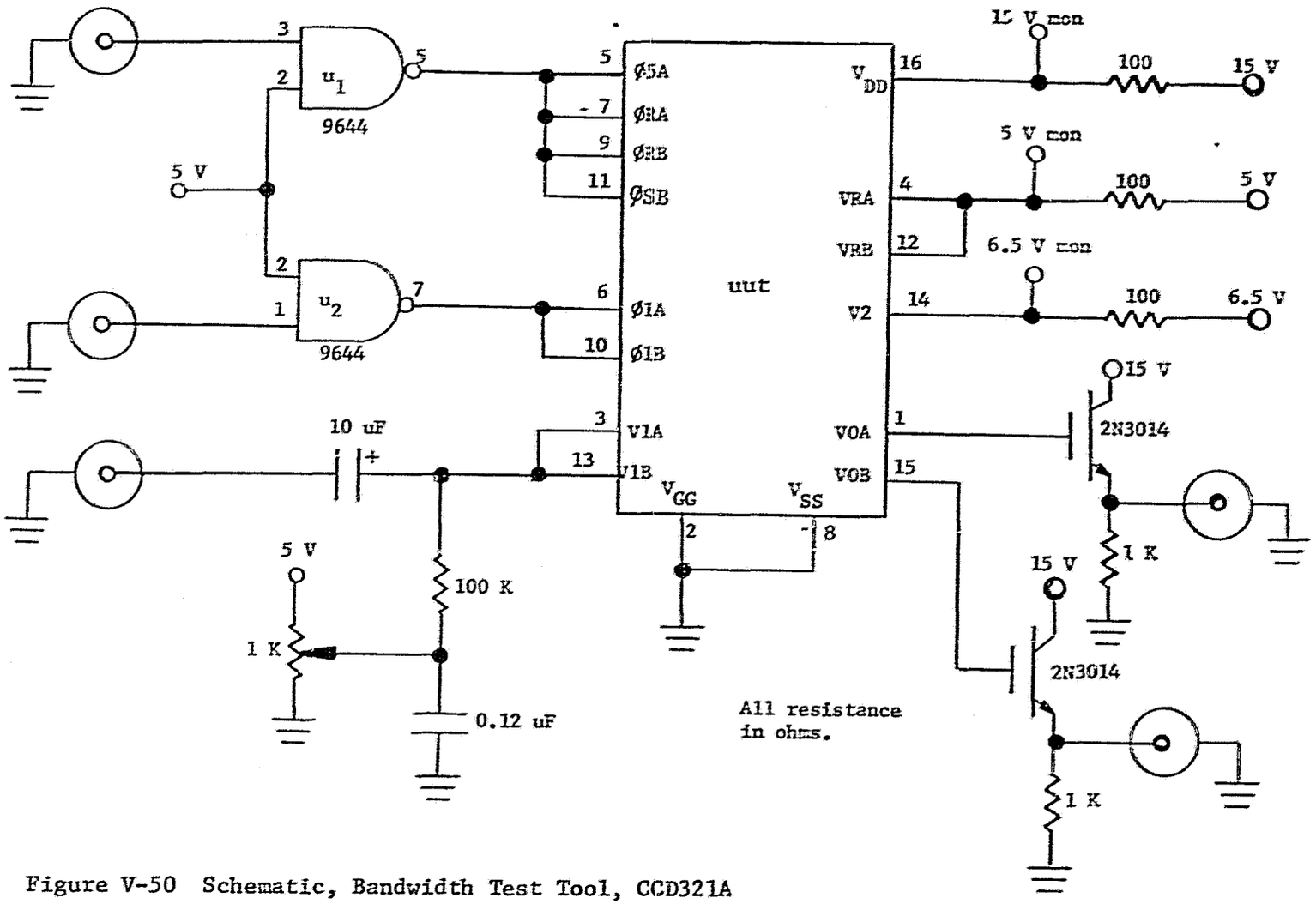


Figure V-50 Schematic, Bandwidth Test Tool, CCD321A

variable frequency sine wave generator, Krohn-Hite Model 2000. The D.C. input level was variable but commonly was set at about 3.3 volts. V_{DD} was adjusted to 15 volts at the unit under test, and VR was set at 5 volts. V2 was originally set at 6.5 volts, however, adjustment of this level was necessary on some of the devices to obtain an undistorted output signal. The outputs were again emitter follower circuits.

The input clock frequency was adjusted to 14.32 MHz. The output level was measured with a 1 volt peak-to-peak sine wave at approximately 700 KHz on the input. The input frequency was then increased until the Nyquist limit was reached. In all cases this occurred prior to the 3db point being reached. The Nyquist limit is equal to one-half of the clock frequency. The sine wave must be sampled at high and low peaks to take this measurement. By adjustment of the input frequency this condition could readily be obtained on the oscilloscope and the output level measured.

g. Transfer Efficiency - This parameter measures the efficiency with which charge is transferred through a device. It is a measurement which shows the difference between a buried-channel device and a surface channel device as discussed previously. It also provides information on several first and second order material and processing effects.

This measurement is made by shifting a charge packet through the device and measuring the output voltage (V1) then switching to no charge being transferred through and measuring this voltage level (V2) and finally measuring the voltage level (V3) which occurs at the single pulse following the change from V1 to V2. The transfer efficiency is then equal to:

$$1 - \left[\frac{V2 - V3}{V1 \times 455}\right]$$

The test tool circuitry was designed to perform these measurements, switches 8 and 9 control the input levels and the counter circuits U13, U14, and U15 control the sample time for the sample and hold circuits. The critical timing for this test is to read the voltage level V3 which occurs at the single output pulse following the change from charge being transferred through to no charge being transferred. In the test tool with switch 9 at ground and switch 8 at 5 volts the input of the CCD321A-2 is 2.87 volts. This provides the output level V1 of about 8.40 volts. To measure V2 with no charge being transferred through, 4.85 volts is applied

to the CCD321A-2. This is accomplished by taking both switch 8 and switch 9 to 5 volts. The output level produced is 9.80 volts. The V3 measurement is taken by setting switch 9 to 5 volts and switch 8 to U19-10. In this configuration the input to the CCD321A-2 is switching between the 2.87 volt input level and the 4.85 volt input level. When the input switches from the 2.87 volt level to the 4.85 volt level the counters reset and count to 455, since this is a 455-stage shift register. The counter circuitry then provides a pulse that is used to control the timing for the sample and hold circuits. The CCD321A-2 output and the timing pulse for the first sample and hold circuit is shown in Figure V-51. The displays have a time base of 10 microseconds per horizontal division, the bottom trace is at 1 volt per vertical division, and the top trace is 5 volts per vertical division. There is little perceptible difference between this first level and subsequent levels. This is approximately 30 mV.

C. Initial Electrical Characterization

The test flow is shown in Figure V-52. The results described are for the third Fairchild lot only.

Initial electrical characterization on the CCD321A-2 devices was performed as described in the previous section.

Five devices were tested to determine if a lot related problem existed with these devices. The following sequence of tests was performed: electrical characterization, environmental screen, and electrical characterization. Leakage current testing was performed first with Serial Number 6 having 1.4 nA leakage. The remainder of the electrical tests were then run followed by a repeat of the leakage current test. S/N6 had increased slightly to 2.2 nA. The parts were then subjected to the environmental screen tests, interim electricals, 160 hour burn-in, and full electrical characterization. The parts continued to operate properly with no increase in leakage. The remainder of the parts were then tested.

Due to the leakage current problems experienced previously, the first incoming electrical to be performed was a current leakage test. S/N 19 was found to have Pin 9 shorted. No other devices exhibited leakage current. The leakage current measurements taken during the course of this testing are shown in Table V-4. These readings are given as a voltage across a 100 kohm current limiting resistor. Therefore 1 volt is equal to 10 microamps.

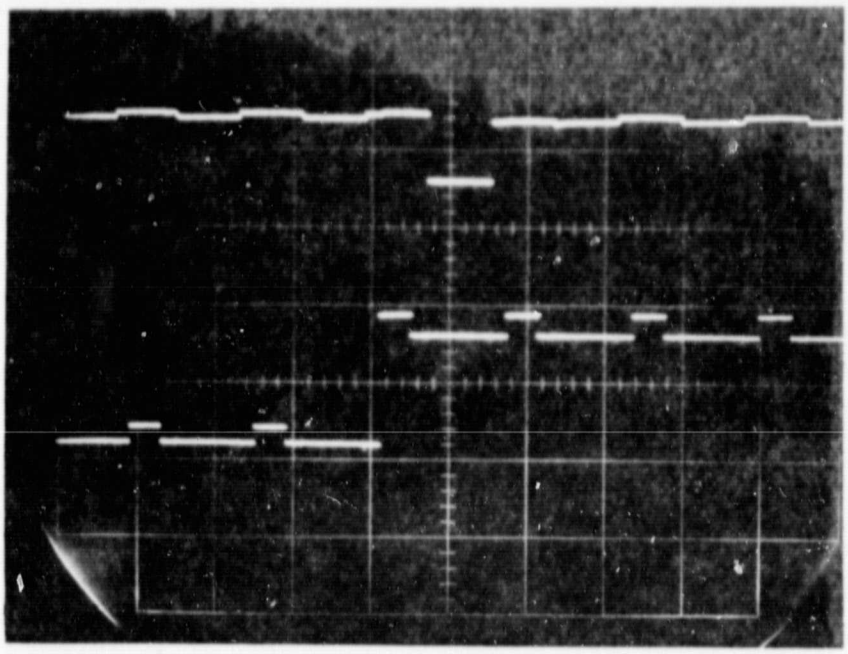


Figure V-51 Output Waveshape for Transfer Efficiency Measurement, CCD321A

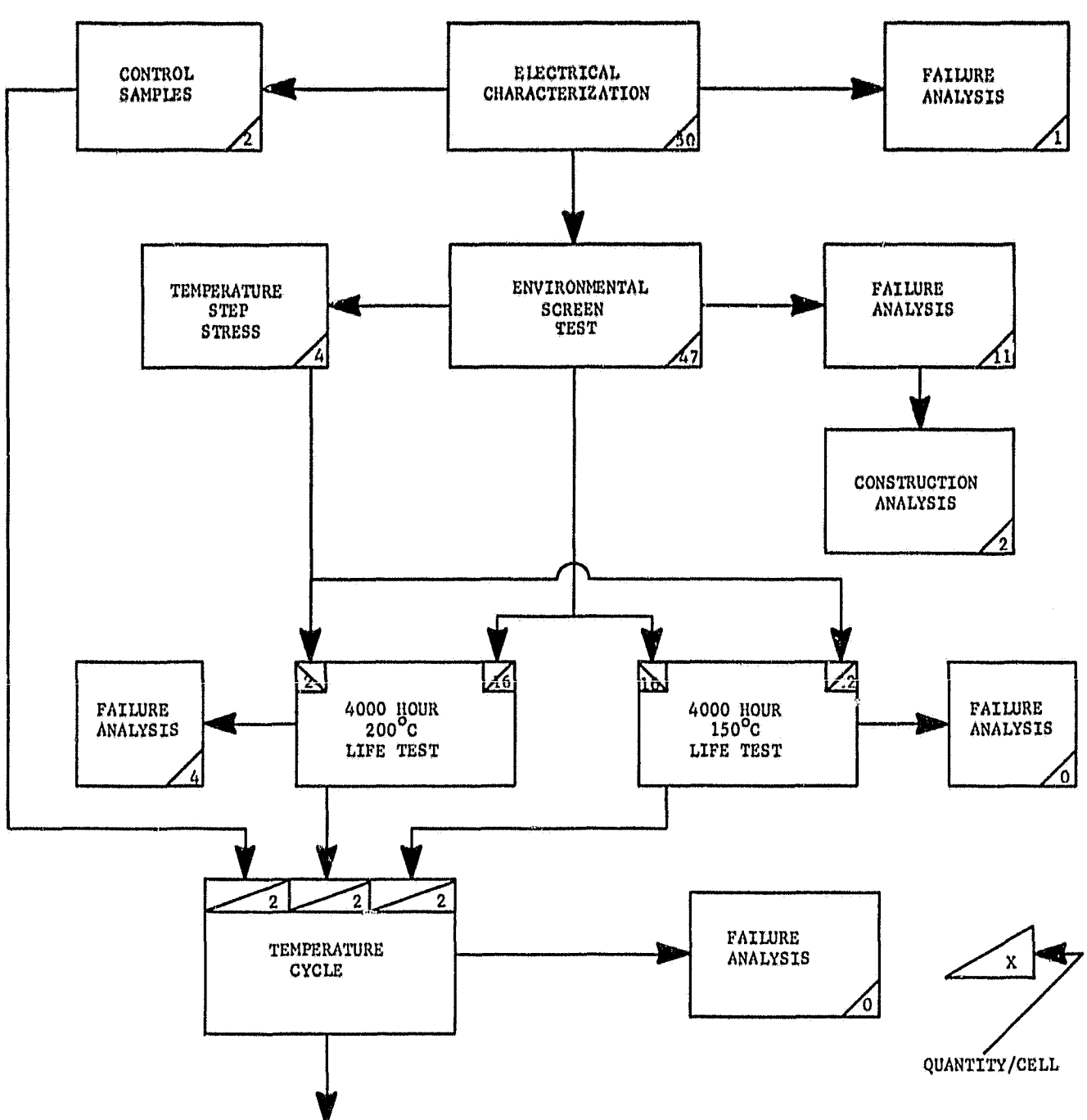


Figure V-52 Test Flow Diagram, Fairchild CCD321A/ Quantities Used

Table V-4 Leakage Measurements, CCD321A (Leakage(uA) = Reading X 10)

Initial meas.	Post initial elect.	Post sta. bake & temp. cycle	Post accel. & seal	Post constant burn-in	Post 160 hr. elect. following 160 hour burn-in		Serial Number	Pin Number	
.0001	.0002	-	-	-	-		6	9	
-	-	-	.0543	pulled			8	9	
-	10.7	10.7	3.8	pulled			14	7	
-	.0015	10.7	2.3	pulled			17	7	
10.3	pulled						19	9	
-	-	-	.1300	pulled			21	12	
-	.0403	.0067	.0182	.0099	.0099		23	7	
-	2.8	2.8	2.8	pulled			24	9	
-	.0096	.0010	.0010	.0009	.0010		30	7	
-	.1498	.0440	.0470	.0277	.0277		38	7	
-	-	-	-	-	11.0		41	9	
-	10.9	10.9	10.7	pulled			44	7	
-	.0099	.0013	.0013	pulled			45	7	
-	10.4	10.4	3.4	pulled			45	9	
-	.1193	.0200	.0413	.0220	.0430		46	9	

The devices were then electrically characterized at -25°C, +25°C, and +55°C. A sample of the electrical readings are given in Table V-5. This provides the data taken at three temperatures on the test tool. Delta calculations between these initial measurements and later measurements will be discussed in the data analysis section. General observations from this data include: an increase with temperature of gain and noise, a decrease with temperature of device current and transfer efficiency, and the voltage offset was highest at +25°C as previously discussed.

The bandwidth test at all temperatures found the bandwidth only limited by the Nyquist sampling limit. The clocks were operated at 14.32 MHz and the bandwidth measured 7.16 MHz.

Following the electrical tests the leakage current was remeasured. The results are again shown in Table V-4. Several more devices are leaky at this point. If fallout were to continue at this rate the test would be terminated.

Serial numbers 1 and 2 were held for controls. The remaining devices were subjected to the environmental screening tests.

D. Environmental Screen

The environmental screen tests were selected from MIL-STD-883, Method 5004, Class B. These tests were previously listed in Table IV-8.

The first screen test was high-temperature storage per Method 1008.1, Condition C. This is a storage temperature of 150°C for 24 hours in a non-powered condition. This stress is used in the screening sequence as a pre-conditioning treatment prior to the following tests.

The second environmental screen test was temperature cycling per Method 1010.2. This is an automated test which exposes the parts to -65°C and +150°C taking 30 minutes per temperature cycle. There was a total of 10 cycles.

At this point a current leakage test was performed. The results are shown in Table V-4. No additional parts became leaky.

The third screen test was constant acceleration per Method 2001.2, Test Condition E. This is a 30,000 g acceleration in the Y1 axis. The Y1 orientation is defined as that one in which the element tends to be removed from its mount. The parts were held in plastic carriers to avoid bending of the external leads.

The fourth screen test was a seal test per method 1014.2. The fine leak test is per Test Condition A1, using helium tracer gas with a bomb time of 2 hours at 60 PSIG. The gross leak test is per Test Condition C, using fluorocarbon.

Table V-5 Initial Electrical Characterization, CCD321A

Parameter	Test Conditions		Spec. Limits Typical[2]	Units	Serial Number 1	3	5
Device Current	Note 1	-25°C	-	mA	6.73	6.62	6.89
		+25°C			5.47	5.44	5.69
		+55°C			4.73	4.74	4.91
Gain Side A	Note 1 Delta V_{IN} = 0.4 V	-25°C	-	V/V	1.10	1.10	1.14
		+25°C			1.11	1.11	1.21
		+55°C			1.11	1.11	1.23
Gain Side B	Note 1 Delta V_{IN} = 0.4 V	-25°C	-	V/V	1.08	1.09	1.16
		+25°C			1.09	1.10	1.20
		+55°C			1.09	1.09	1.21
Offset Voltage Side A	Note 1 V_{IN} = 5.0 V	-25°C	-	V	9.50	9.51	9.46
		+25°C			9.59	9.61	9.37
		+55°C			9.35	9.39	9.05
Offset Voltage Side B	Note 1 V_{IN} = 5.0 V	-25°C	-	V	9.49	9.50	9.64
		+25°C			9.58	9.60	9.64
		+55°C			9.37	9.41	9.39
Noise Side A	Note 1 V_{IN} = 3.9 V	-25°C	-	mV	0.35	0.21	0.26
		+25°C			0.25	0.27	0.94
		+55°C			0.65	0.57	0.77
Noise Side B	Note 1 V_{IN} = 3.9 V	-25°C	-	mV	0.36	0.65	0.39
		+25°C			0.26	0.25	0.39
		+55°C			0.57	0.63	0.61
Transfer Eff. Side A	Note 1	-25°C	-		1.0	1.0	.999990
		+25°C			.999997	.999996	.999974
		+55°C			.999988	.999988	.999964
Transfer Eff. Side B	Note 1	-25°C	-		1.0	1.0	.999991
		+25°C			.999997	.999997	.999987
		+55°C			.999990	.999989	.999975

Note 1 - V_{DD}=15 V, sampling frequency = 62.5 KHz.

Note 2 - No specifications available.

Interim electrical tests were performed at this time. This testing is used to verify the functionality of the devices and provide information on the effect of the preceding tests on parameter stability. The data was stored on tape and comparison was made with the initial measurements.

Parts which exhibited high leakage currents and significant shifts in their parameters were removed at this time. This included serial numbers 8, 9, 14, 17, 21, 24, 43, 44 and 45. At this time overvoltage testing was performed on some of these devices to determine the breakdown level of the oxide. In addition to the above parts, S/N 1 was also tested. The voltage on pin 7 with respect to ground was raised to 28 volts. The oxide broke down at this point and the part was now an electrical failure. Due to this overstress S/N 3 was relabeled as S/N 1 and used for a control during the remainder of the test.

The fifth screening test was the 160 hour burn-in at 55°C. This is the maximum specified operating temperature for this device and it was used since the effects of higher temperature operation were unknown at this point.

Following this 160 hour burn-in the parts were again electrically characterized. There was one additional part which was leaky on pin 9, S/N 41. This device was removed from test. Serial numbers 23, 30, 38 and 46 had exhibited low level leakage current, however, no change in their electrical parametrics had been observed so they were left in test.

E. Thermal Step Stress Test

This test was performed to establish the temperatures used in the 4,000 hour life test. The circuit used is the same one as that to be used for the life test.

The test plan is the same as that used for the Reticon devices and is repeated below:

1. Operate four circuits for 16 hours at +65°C. Monitor the outputs for functionality and record the power supply currents at the start and end of test.

2. Perform the interim electrical tests at +25°C.

3. Increase the operating temperature in 10°C increments until malfunction or permanent parameter shift occurs. Malfunction is defined as the point where the output, which has previously saturated, no longer exhibits a regular time sampled analog pulse train. Other malfunction criteria is any significant shift in current at temperature.

The power supply currents were monitored during the course of this testing as noted. There was no change in the supply currents except for a gradual decrease in the current on the 15 volt supply. This is the output amplifier voltage source. The current decreased in an approximately linear fashion from 23 mA at 65°C to 14.5 mA at 215°C. The appearance of the output waveform over temperature is shown in Figures V-53 to V-57. The small white bar in the lower left hand corner indicates the ground level. These photographs are taken with the vertical scale at 2 volts per division and the time base at 200 microseconds per division. From this series of photographs it is apparent that the output which started as basically a square wave degrades to a line with a short duration pulse at 200°C.

The interim electricals taken after each 10°C stress are shown in Table V-6. All devices had a decrease in the supply current with stress time. There was also a gradual shift in the other parameters with stress, however, there were no significant changes. One device with a leakage current condition was subjected to the step stress test. The voltage level readings related to the leakage current are shown in Table V-6d. These levels decreased during the course of the test.

From the output waveform appearance, the electrical data, and the failure rate experienced during the Reticon life test the temperatures for the 4,000 hour life test were selected. The lower temperature selected was 150°C. The output waveform is not flat at this point and higher current is flowing in the amplifier section. The upper temperature selected was 200°C. This was the highest practical temperature which could be used for a long term life test with the burn-in boards and ovens available.

F. High Temperature Life Test

The burn-in circuit used for the life test is shown in Figure V-58. The voltages applied to the device are as shown. Pin 1 is the side A output and it is wired to the outside for monitoring. Pins 5, 7, 9 and 11 are connected to a 1.1 KHz waveform that is identical in shape to that used in the test tool. This input goes high for 225 microseconds during the middle of the period that Ø1 is low. Ø1 is a square wave at 1.1 KHz and goes to pins 6 and 10. Both of these waveforms go from 0 to 15 volts. The monitor points were checked daily to verify proper operation. The analog inputs, pins 3 and 13 are at 3 volts. A zener overvoltage protection diode and a 9 kohm current limiting resistor are in this circuit. The voltage level monitoring points were also checked on a daily basis. The reference voltage input, pins 4 and 12, are at 5 volts. This line is again protected with a zener diode and a current limiting resistor. The charge input is related to the

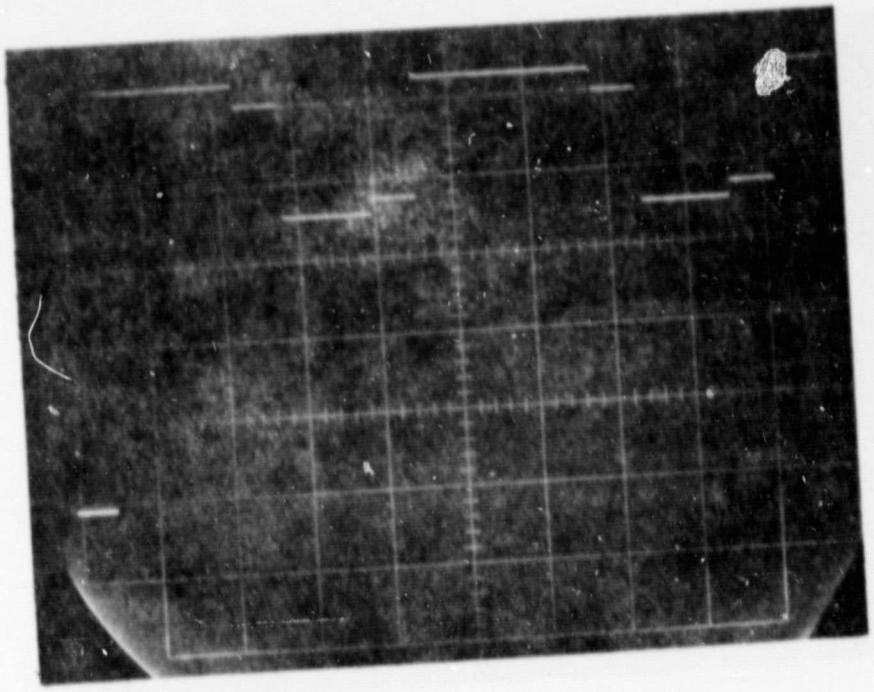


Figure V-53 Output Waveform, 25°C, CCD321A

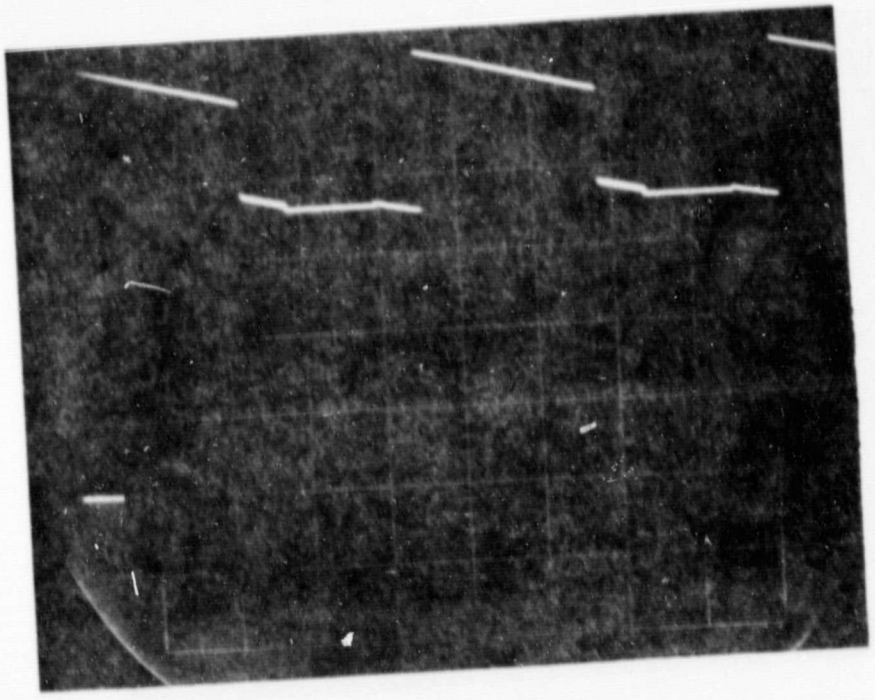


Figure V-54 Output Waveform, 125°C, CCD321A

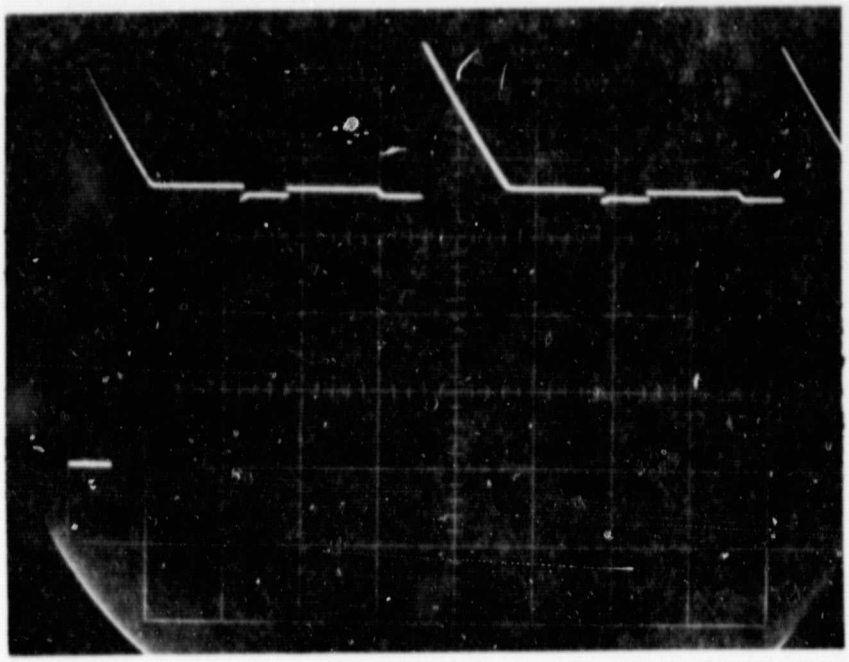


Figure V-55 Output Waveform, 150°C, CCD321A

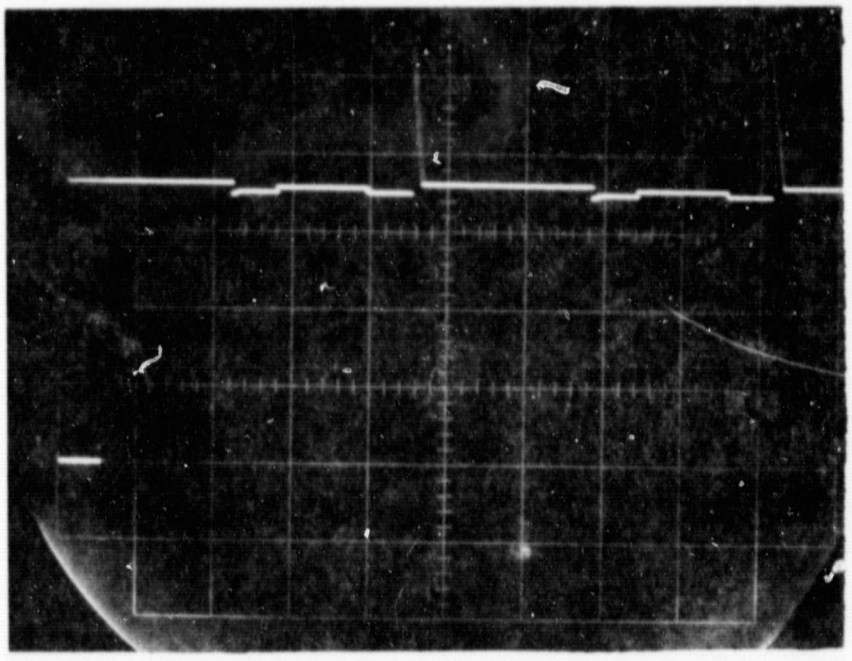


Figure V-56 Output Waveform, 175°C, CCD321A

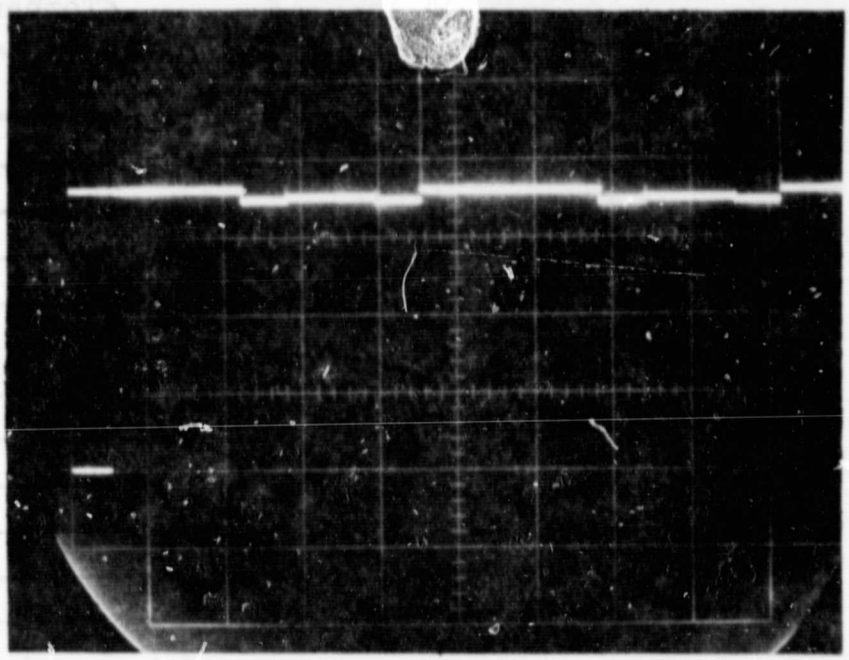


Figure V-57 Output Waveform, 200°C, CCD321A

Table V-6a Step Stress Electricals, S/N 35, CCD321A

Device Current (mA)	Gain (V/V) Side A	Gain (V/V) Side B	Offset Voltage (V) Side A	Offset Voltage (V) Side B		Stress Temperature (°C)	
6.65	1.11	1.12	10.01	10.09		65	
6.63	1.11	1.12	10.00	10.09		75	
6.61	1.11	1.12	10.02	10.10		85	
6.59	1.11	1.13	10.03	10.11		95	
6.53	1.11	1.12	10.03	10.12		105	
6.61	1.11	1.13	10.03	10.11		115	
6.63	1.10	1.12	10.06	10.12		125	
6.58	1.10	1.12	10.06	10.12		135	
6.64	1.10	1.12	10.06	10.12		145	
6.57	1.10	1.11	10.07	10.12		155	
6.53	1.10	1.12	10.07	10.13		165	
6.53	1.10	1.12	10.09	10.12		175	
6.54	1.10	1.13	10.09	10.11		185	
6.49	1.11	1.13	10.09	10.11		195	
6.49	1.11	1.13	10.08	10.10		205	
6.48	1.11	1.13	10.09	10.10		215	

Table V-6b Step Stress Electricals, S/N 36, CCD321A

Device Current (mA)	Gain (V/V) Side A	Gain (V/V) Side B	Offset Voltage (V) Side A	Offset Voltage (V) Side B		Stress Temperature (°C)	
6.21	1.25	1.23	9.90	9.91		65	
6.18	1.25	1.23	9.91	9.92		75	
6.16	1.25	1.23	9.91	9.92		85	
6.18	1.25	1.23	9.93	9.93		95	
6.13	1.25	1.23	9.93	9.93		105	
6.16	1.25	1.23	9.93	9.93		115	
6.18	1.24	1.23	9.95	9.93		125	
6.16	1.23	1.23	9.95	9.93		135	
6.18	1.24	1.23	9.94	9.92		145	
6.16	1.23	1.23	9.95	9.92		155	
6.05	1.24	1.24	9.96	9.94		165	
6.12	1.24	1.24	9.95	9.92		175	
6.14	1.24	1.24	9.94	9.91		185	
6.08	1.24	1.24	9.94	9.91		195	
6.04	1.24	1.25	9.94	9.91		205	
6.03	1.24	1.25	9.94	9.90		215	

Table V-6c Step Stress Electricals, S/N 37, CCD321A

Device Current (mA)	Gain (V/V) Side A	Gain (V/V) Side B	Offset Voltage (V) SideA	Offset Voltage (V) Side B		Stress Temperature (°C)	
3.94	1.17	1.15	9.46	9.75		65	
3.93	1.16	1.15	9.48	9.76		75	
3.91	1.16	1.15	9.50	9.77		85	
3.91	1.14	1.14	9.56	9.80		95	
3.92	1.15	1.14	9.55	9.80		105	
3.91	1.14	1.14	9.57	9.81		115	
3.92	1.13	1.13	9.61	9.82		125	
3.91	1.12	1.13	9.62	9.83		135	
3.93	1.12	1.13	9.60	9.81		145	
3.92	1.12	1.13	9.62	9.82		155	
3.86	1.12	1.13	9.63	9.83		165	
3.89	1.12	1.13	9.62	9.82		175	
3.91	1.14	1.14	9.53	9.77		185	
3.86	1.11	1.12	9.61	9.81		195	
3.86	1.11	1.12	9.61	9.80		205	
3.86	1.11	1.12	9.61	9.80		215	

Table V-6d Step Stress Electricals, S/N 38, CCD321A

Leakage Current $I=V/10^5$ (V)	Device Current (mA)	Gain (V/V) Side A	Gain (V/V) Side B	Offset Voltage (V) Side A	Offset Voltage (V) Side B		Stress Temperature (^oC)	
.0265	6.10	1.23	1.21	9.95	9.90		65	
.0253	6.07	1.23	1.21	9.95	9.90		75	
.0230	6.05	1.23	1.21	9.96	9.90		85	
.0161	6.04	1.23	1.21	9.97	9.92		95	
.0151	5.98	1.23	1.21	9.96	9.91		105	
.0131	6.04	1.23	1.21	9.97	9.91		115	
.0112	6.03	1.23	1.21	9.97	9.92		125	
.0090	6.01	1.22	1.21	9.97	9.91		135	
.0079	6.09	1.23	1.21	9.96	9.90		145	
.0051	6.04	1.22	1.20	9.97	9.91		155	
.0044	6.02	1.23	1.21	9.98	9.92		165	
.0037	5.98	1.23	1.21	9.97	9.91		175	
.0023	6.03	1.23	1.21	9.96	9.89		185	
.0019	5.97	1.23	1.21	9.96	9.89		195	
.0017	5.91	1.23	1.21	9.96	9.89		205	
.0015	5.88	1.24	1.22	9.96	9.89		215	

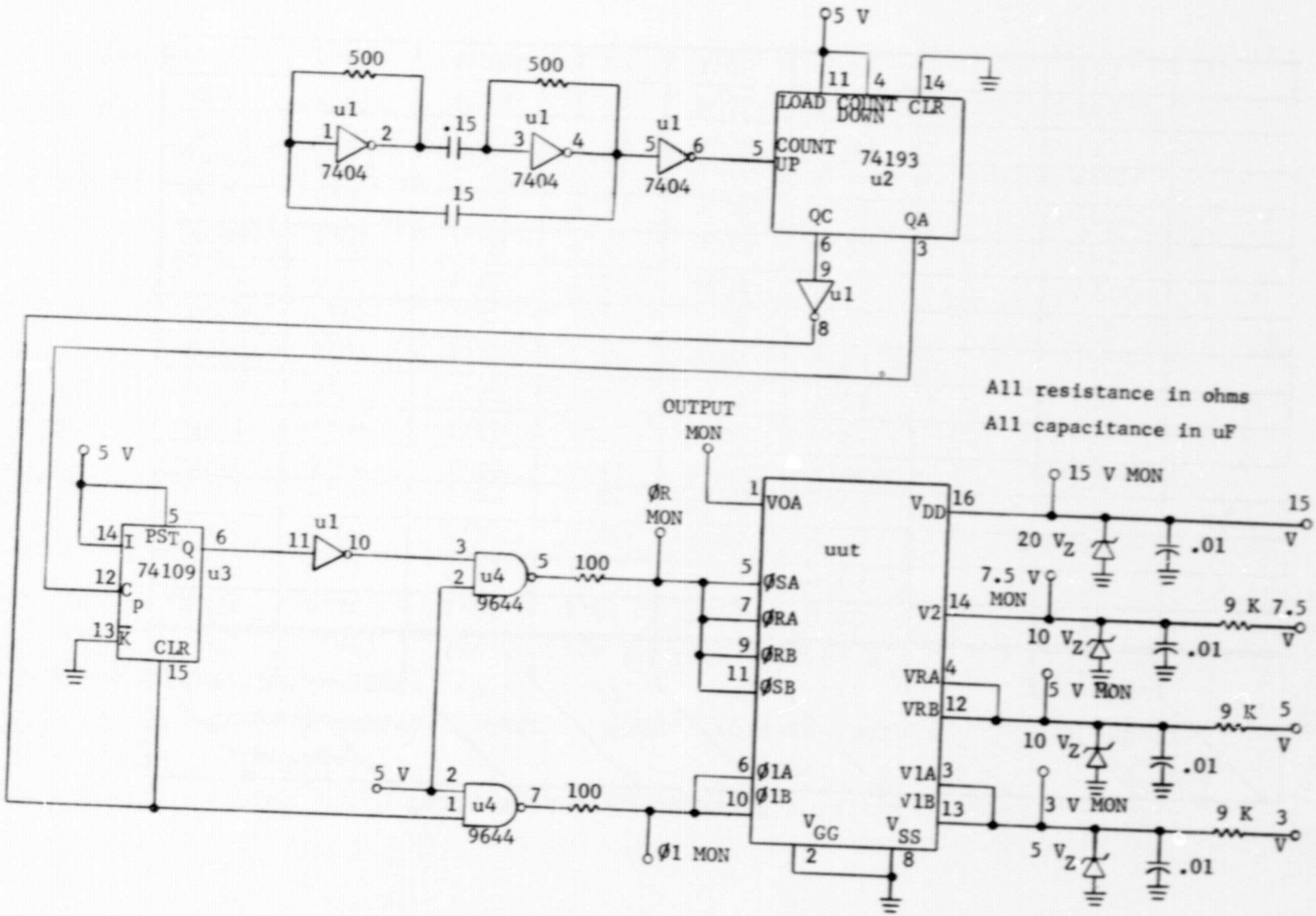


Figure V-58 Life Test Burn-in Circuit, CCD321A

difference between the reference voltage input and the analog voltage input. This voltage difference is two volts and therefore there is charge being supplied by the input circuit. The V2 input, pin 14, is held at one-half of the clock voltage level. This is 7.5 volts and again a zener diode and current limiting resistor are in the circuit. The VDD line, Pin 16, is held at 15 volts. The power supply is set in current limiting when the parts have stabilized at temperature. There is a 20 volt zener protect diode on this line. Signal ground and substrate ground pins 2 and 8 are connected together and tied to a common ground.

With the fallout which had occurred prior to this point there were 38 parts remaining for the life test. Two of these were control parts and the remaining 36 devices were divided into two groups for the life test.

S/N 4, 5, 6, 7, 10, 11, 12, 13, 15, 16, 18, 20, 22, 23, 25, 26, 27 and 28 were operated at 150°C. S/N 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 42, 46, 47, 48, 49 and 50 were operated at 200°C.

Interim electrical measurements were made at 4, 8, 16, 32, 64, 128, 256, 500, 1,000 and 2,000 hours. Full electricals were made at 4,000 hours cumulative. The output of each circuit and the monitor points were checked daily. The current level on each power supply was read and recorded at the beginning and end of each period of test. The 15 volt supply on the 150°C burn-in oven drew about 58mA and the 200°C burn-in oven drew about 48mA initially and about 39mA at the end of the test. The change in current level on the 200°C burn-in test was due to device failures during the test.

The devices which were removed during the test were serial number 49 following 64 hours of operation, serial numbers 36 and 46 following 256 hours of operation, and serial number 40 following 500 hours of operation. A complete analysis of these circuits is covered in the failure analysis section. A brief summary is given here: S/N 49 and S/N 40 failed due to ionic contamination, S/N 36 failed due to a metallization fault, S/N 46 failed due to a layer-to-layer short. S/N 46 had leakage from the start of the life test and it finally degraded to failure.

The parts which exhibited leakage current during the life test are shown in Table V-7. S/N 6 was the only device which became leaky during the life test. This part had on the order of 2 nanoamps of leakage. An additional pin on S/N 23 was found to be leaky after 1,000 hours of life test. The leakage on S/N 38 became significantly worse during the last 2,000 hours of operating test. The results of this leakage current change with long term stress indicates that this is not a time-temperature accelerated failure mechanism.

Data analysis on these parts is included in the data analysis section.

TABLE V-7 DEVICE LEAKAGE (V); 321A

TEST HOURS	SERIAL NO - PIN NO					
	6-9	23-7	23-9	30-7	38-7	46-9
4	-	.0036	-	.0004	.0015	.0037
8	-	.0030	-	.0004	.0015	.0035
16	-	.0024	-	.0002	.0015	.0033
32	-	.0020	-	.0002	.0014	.0030
64	.0003	.0017	-	.0002	.0014	.0030
128	.0002	.0014	-	.0002	.0013	.0033
256	.0002	.0011	-	.0001	.0012	10.9
500	.0002	.0011	-	.0001	.0011	PULLED
1000	.0002	.0008	.0206	.0001	.0014	-
2000	.0001	.0006	.0007	.0014	.0000	-
4000	.0001	.0005	.1071	.0000	2.2	-

G. Temperature Cycle

At the completion of the 4,000 hour life test 6 devices were subjected to 1,000 temperature cycles. Two devices were taken from each of the life test groups and the two control parts were used.

The temperature cycles were performed in accordance with MIL-STD-883, Method 1010, Condition C (150°C to -65°C).

Electrical measurements were taken before temperature cycling and after 20, 50, 250, 500 and 1,000 cycles.

Table V-8 provides the electrical data on these 6 devices and a control part at initial test and following 1,000 cycles.

H. Overvoltage Test

Six units were subjected to overvoltage conditions on various pin combinations to determine whether there were any combinations which resulted in permanent damage to the devices. The pins selected included input gates to substrate and overlapping polysilicon layers. The following pin combinations were stressed on each of the six devices: 5 to 3, 3 to 5, 4 to 5, 5 to 4, 4 to 6, 6 to 4, 6 to 14, 14 to 6, 4 to 2, 4 to 8, 6 to 2, 6 to 8, 14 to 2, 14 to 8, 7 to 16, 7 to 2, 7 to 8, 11 to 13, 13 to 11, 12 to 11, 11 to 12, 12 to 10, 10 to 12, 10 to 14, 14 to 10, 12 to 2, 12 to 8, 10 to 2, 10 to 8, 9 to 16, 9 to 2, and 9 to 8. These were stressed with the first pin being positive with respect to the second. The breakdown voltages on these pins was normally 35 volts. Two devices did fail during this test. S/N 30 failed at 20 volts between pins 7 and 2. This is the type of layer-to-layer short which has been seen previously on these devices. S/N 6 had approximately 1nA of leakage going into this test. It failed at about 25 volts between pins 9 and 2. Again this is the same type of failure.

The remaining four devices were subjected to short circuit output conditions. The input was set to obtain maximum output current and then the output was shorted to ground. The current flow was between 19 and 25 mA. One unit was left in a shorted condition for 45 minutes with no degradation occurring.

The final stress test was to apply overvoltage conditions to the input and output circuits. The input circuits were taken to greater than 100 volts with no failures occurring. The output circuits would fail with stress applied between the output pin and V_{GG} or between V_{DD} and V_{GG}. These pin combinations went into breakdown at about 30 volts and then a negative resistance type characteristic similar to a BV_{CEO} curve occurred. The output would fail at about 80mA current flow. The voltage at that point was about 10 volts.

Table V-8 Temperature Cycle Electricals, CCD321A

Device Current (mA)	Gain V/V Side A	Gain V/V Side B	Offset Voltage (V) Side A	Offset Voltage (V) Side B		Serial Number	Time of measurement	
5.25	1.21	1.21	9.80	9.85		control	initial	
5.31	1.20	1.21	9.80	9.84		control	final	
5.53	1.11	1.10	9.58	9.58		1	initial	
5.64	1.11	1.10	9.56	9.55		1	final	
6.63	1.09	1.10	9.99	10.03		2	initial	
6.74	1.09	1.10	9.95	10.00		2	final	
6.36	1.22	1.23	9.89	9.86		26	initial	
6.41	1.21	1.22	9.88	9.85		26	final	
3.96	1.11	1.07	9.29	9.29		27	initial	
4.05	1.09	1.07	9.30	9.28		27	final	
6.26	1.27	1.26	10.09	10.08		48	initial	
6.37	1.27	1.25	10.07	10.06		48	final	
5.47	1.20	1.21	9.89	9.88		50	initial	
5.57	1.20	1.21	9.86	9.86		50	final	

The two devices which had their output circuitry overstressed were opened and examined. There was no evidence of the failure sites. This is due to the fact that the failures would be hidden beneath the gate polysilicon. The parts were not chemically stripped to view these sites since this type of failure is not typical of that expected.

I. Data Analysis

This section will include a discussion of the deltas which occurred during the course of this testing and statistics on each of the parameters measured. Life regression curves were not generated due to the small number of failures which occurred.

Electrical measurements were run at +25 °C, -25 °C, and +55 °C during the initial characterization and following the environmental screen tests. Table V-9 lists the TCNs upon which data analysis was performed.

Table V-10 lists the deltas between the initial measurements and the post environmental screen measurements at +25 °C.

There was only one control device for these readings as discussed in the environmental screen test section. Two sets of deltas are listed for serial number 2 in Table V-10a. The first set was run at the same time as serial numbers 4 through 7. The second set was used for the remainder of the devices. Serial numbers 4-7 were in the qualification group. Two sets of calculations are provided at the bottom of the page. There was less than 2% change in the readings for I_{DD}, Gain, Offset Voltage and Transfer Efficiency. The noise measurement does not lend itself to delta calculations due to its random nature.

S/N 28 had a gain change of about 25% on side B. This was due to a change in the transfer function on this side. Failure analysis was performed on several similar units and layer-to-layer shorts were identified. This part was left in the life test.

Table V-10b contains the deltas for the parts in the 200 °C life test group.

The changes are again quite small except for the gain on side A on S/N33. Measurement found this part to have leakage between ØR4 and VIA.

The largest transfer efficiency change was 13 x 10^{-6} on S/N25. This is a change of about 50 mV for the V3 reading for transfer efficiency. With V2 equal to 9.8 volts and V1 equal to 8.4 volts this would be a change from 9.52 volts up to 9.57 volts on V3. The available limits of the change which can be seen are 1.0 for V3 = 9.8 and 0.9996 for V3 = 8.4. The change that was seen on this part was from 0.999926 to 0.999939.

Table V-11 contains the delta calculations for the -25 °C measurements. The gain reading for serial number 28 side B, and serial number 33 side A are not utilized for the calculations. The average changes in Table V-11a are very small as are the average changes in Table V-11b.

TABLE V-9 TCN LIST, CCD321A

TCN	SEQUENCE	TEST TEMPERATURE
0	INITIAL	25°C
1	INITIAL	-25°C
2	INITIAL	55°C
4	POST ENVIRON	25°C
5	POST ENVIRON	-25°C
6	POST ENVIRON	55°C
117	POST LIFE TEST 150°C	25°C
217	POST LIFE TEST 200°C	25°C

TABLE V-10a MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @25°C; 321A

I_{DD} (mA)	Gain $\times 10^{-4}$ SideA	Gain $\times 10^{-4}$ SideB	Voffset $\times 10^{-4}$ (V) SideA	Voffset $\times 10^{-4}$ (V) SideB	Noise (mV) SideA	Noise (mV) SideB	CTE $\times 10^{-6}$ SideA	CTE $\times 10^{-6}$ SideB	FOR 150°C TEST Serial Numbers
-.02	-9	-36	51	-32	.03	-.25	0	0	2 - Control (for 4-7)
.16	21	47	-192	-191	.05	.18	1	0	2 - Control(for 10-28)
-.08	-86	-71	-41	-28	.04	-.09	1	0	4
-.02	-197	-159	295	221	-.61	0	4	3	5
.06	-34	-34	-60	-133	.01	.11	0	0	6
.03	-177	-132	140	69	-.13	-.23	5	8	7
.04	14	-1	-140	-128	0	-.31	1	0	10
.01	-149	-129	24	2	-.02	-.27	5	3	11
.05	-196	-131	86	15	.01	-.12	8	5	12
.01	-70	-52	20	10	-.02	-.31	4	-1	13
.11	-26	-61	-59	-50	-.22	-.35	2	2	15
0	-116	-85	108	59	-.31	.01	4	3	16
.06	26	119	-73	-88	-.05	.40	0	0	18
0	-130	-96	-97	-75	-.37	-.10	4	3	20
.12	-1	30	-162	-201	.02	.66	1	0	22
.10	-277	-271	236	211	0	-.06	10	10	23
.18	-56	-321	372	318	-.30	-.14	13	10	25
.12	-149	-115	4	-15	.01	.07	3	4	26
.01	-239	-157	535	376	-.09	-.40	9	5	27
-.02	-48	-2767	5	8	-.01	0.10	5	2	28
0	-123	-99	83	32	-.17	-.05	2.5	2.7	Average (4-7)
.06	77	57	167	150	.30	.14	2.4	3.8	Standard Deviation
0.3	-1.0	-0.6	0	0	-40	40	-	-	% CHANGE (CONTROL)
.06	-101	-288	61	23	-.10	-.07	4.9	3.3	Average (10-28)
.06	94	722	198	165	.14	.30	3.8	3.4	Standard Deviation
-1.7	-1.1	6.1	0.3	0.2	-30	-50	-	-	% CHANGE (CHANGE)
6	11000	11000	100000	100000	.50	.50	999999	999999	Typical Value

TABLE V-10b MEASUREMENT DELTAS, INITIAL @ POST ENVIRON. @ 25°C; 321A

IDD	Gain $\times 10^{-4}$	Gain $\times 10^{-4}$	V-offset $\times 10^{-4}$	V-offset $\times 10^{-4}$	Noise (mV)	Noise (mV)	CTE $\times 10^{-6}$	CTE $\times 10^{-6}$	FOR 200°C TEST Serial Number
.16	21	47	-192	-191	.05	.18	1	0	2 - Control
-.07	-6	41	-2	-21	-.02	-.62	1	1	29
.06	-65	-72	-134	-96	-.57	.10	2	2	30
.02	-155	-72	304	159	-.50	-.31	6	3	31
.05	-175	-51	53	-56	-.05	-.15	5	1	32
.09	-2259	-169	55	38	.02	-.01	5	5	33
.10	-88	-79	-27	-148	0	-.36	3	2	34
0	-69	-7	153	80	-.03	0	2	1	35
0	-133	-97	119	21	-.01	-.10	5	3	36
.06	133	-68	273	86	-.25	.05	4	2	37
-.08	-116	-217	-13	14	.02	-.21	2	1	38
0	-129	-67	339	232	-.03	.01	4	3	39
.09	-89	-176	190	89	.03	-.02	3	2	40
.12	125	20	-364	-192	0	.45	1	1	42
-.02	-20	-28	-101	107	-.03	-.49	1	2	46
.09	-205	-109	434	171	-.06	.33	9	4	47
.01	-61	-56	20	44	-.03	-.42	3	2	48
-.03	-246	-97	499	196	-.25	-.40	8	3	49
-.08	2	-5	-39	-11	.05	-.41	1	0	50
.02	-198	-73	97	40	-1.0	-.14	3.6	2.1	Average
.06	524	67	216	116	.18	.29	2.4	1.2	Standard Deviation
-2.3	-2.0	-1.1	0.3	0.2	-30	-64	-	-	% CHANGE (CONTROL)
6	11000	11000	100000	100000	.50	.50	999999	999999	Typical Value

TABLE V-11a MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ -25°C

IDD (mA)	Gain $\times 10^{-4}$ SideA	Gain $\times 10^{-4}$ SideB	V- offset $\times 10^{-4}$ SideA	V- offset $\times 10^{-4}$ SideB		FOR 150°C TEST Serial Number
.08	-22	-31	-155	-283		2 - Control (for 4-7)
.13	52	56	-46	-32		2 - Control
.07	-72	-84	-190	-139		4
.05	-145	-161	-128	-67		5
.06	-16	-32	-170	-153		6
.04	-141	-175	-221	-64		7
.05	54	61	-80	-71		10
.03	-2	38	-28	-110		11
.05	-29	4	56	20		12
.04	33	17	25	26		13
0	78	68	-59	-43		15
.02	-15	24	-12	7		16
.04	114	274	-8	8		18
-.02	-5	24	48	48		20
.02	92	14	-103	-87		22
.04	0	30	-103	-102		23
.02	227	-93	11	44		25
-.08	-63	9	-224	-226		26
-.03	-1	17	-526	-363		27
-.02	177	5823	-186	-126		28
.06	-93	-113	-177	-106		Average (4-7)
.01	62	67	39	47		Standard Deviation
-0.3	-0.6	-0.7	0	0.2		% CHANGE (CONTROL)
.01	47	37	-85	-70		Average (10-28)
.04	82	81	152	115		Standard Deviation
-1.7	0	-0.2	0	0		% CHANGE (CONTROL)
7	11000	11000	95000	95000		Typical Value

TABLE V-11b MEASUREMENT DELTAS, INITIAL & POST ENVIRON. @ -25°C

IDD (mA)	Gain $\times 10^{-4}$ SideA	Gain $\times 10^{-4}$ SideB	V- offset $\times 10^{-4}$ SideA	V- offset $\times 10^{-4}$ SideB		FOR 200°C TEST Serial Number
.13	52	56	-46	-32		2 - Control
-.02	30	88	-109	-110		29
.03	85	59	-183	-138		30
.03	81	165	-333	-243		31
.03	-20	-3	-81	-70		32
.01	3037	30	-61	-22		33
0	52	34	-133	-104		34
0	75	250	-98	-48		35
.03	37	15	-103	-79		36
-.03	573	42	-371	-333		37
0	-115	-153	-399	-359		38
0	-33	-20	-409	-437		39
-.02	-115	-154	-432	-420		40
-.01	172	34	-577	-364		42
-.03	-81	-36	-375	-320		46
.04	-182	-137	-202	-327		47
.02	-52	-109	-364	-363		48
0	-129	-95	-312	-333		49
.01	-48	-51	-329	-325		50
.005	19	-3	-271	-244		Average
.02	170	108	151	141		Standard Deviation
-1.8	-0.3	-0.5	-0.2	-0.2		% CHANGE (CONTROL)
7	11000	11000	95000	95000		Typical Value

A ten percent change in each of these readings would be as follows: I_{DD} = 0.7 mA, Gain = 1100 x 10^{-4}, and Voffset = 95000 x 10^{-4}. With the exception of serial numbers 28 and 33 none of the parts approach these levels.

Table V-12 contains the delta calculations for the +55°C readings. Again S/N 28 and 33 are not used to calculate the average changes.

The changes which occur in Tables V-10, V-11, and V-12 are small and in no specific direction. The changes of the parts with operating life will provide a better data base for information on the stability of this technology.

For the 4000 hour life test there were two control parts utilized. The deltas for these control parts and for the test units are given in Table V-13.

A comparison of the data on Table V-13a and V-13b provides some interesting information. The standard deviations on these tables are very large which indicates a wide variation in the amount of change which has occurred. The average changes are fairly small, with the 150°C test group, Table IV-13a being smaller than the 200°C test group, Table IV-13b.

The numeric change in I_{DD} was small with approximately .01 to .02 mA being the most frequently occurring value on the 150°C group. The change in I_{DD} on the 200°C group is most frequently in the -0.10 mA range. This is larger and in the opposite direction.

The change in gain was commonly about -2% on the 150°C group and about +3% on the 200°C group.

The Voffset changes are of about equal magnitude both positive and negative for the 150°C group. This measurement was normally a positive change of about 1% on the 200°C group.

The noise measurements showed some shift in the positive direction, however, this is a difficult measurement to obtain good statistical data.

The last measurement, transfer efficiency, showed a consistent increase for the 150°C group and a consistent decrease for the 200°C group.

It has been reported that hot electron injection causes a degradation of transfer efficiency at high temperature. Since there are two distinct characteristics shown by this data, there is an effect on the CCDs related to high temperature. The minimum temperature required to produce this effect is between 150°C and 200°C.

TABLE V-12a MEASUREMENT DELTAS, INITIAL @ POST ENVIRON.

IDD (mA)	Gain $\times10^{-4}$ SideA	Gain $\times10^{-4}$ SideB	V-offset $\times10^{-4}$ SideA	V-offset $\times10^{-4}$ SideB	@ 55°C; 321A FOR 150°C TEST Serial Number
-.03	3	-53	-68	-207	2 - Control(for 4-7)
.05	0	-57	-285	-470	2 - Control(for 10-28)
-.02	-15	-20	-161	-95	4
.01	-214	-146	71	48	5
0	-43	-23	-134	-121	6
-.03	-100	-80	-362	-195	7
-.02	-11	55	64	11	10
-.02	-287	-90	-740	-902	11
.02	-230	-113	255	167	12
.02	-173	-114	-78	-143	13
.01	-131	-32	165	127	15
0	-202	-69	175	101	16
0	-11	122	289	217	18
.03	-266	-160	-61	-118	20
-.01	-11	64	52	58	22
-.03	-234	-108	304	217	23
0	-13	-173	319	352	25
.06	-187	-170	89	99	26
-.01	-276	-69	491	269	27
.04	-238	-2252	497	425	28
-.01	-93	-67	-146	-91	Average
.02	88	59	177	102	Standard Deviation
0.4	-0.9	-0.1	0	0.1	% CHANGE (CONTROL)
.01	-161	-66	130	61	Average
.02	108	94	307	320	Standard Deviation
-0.8	-1.5	0	0.4	0.8	% CHANGE (CHANGE)
5	11000	11000	95000	95000	Typical Value

TABLE V-12b MEASUREMENT DELTAS, INITIAL & POST EVIRON. @ 55°C;

IDD (mA)	Gain $x10^{-4}$ SideA	Gain $x10^{-4}$ SideB	V- offset $x10^{-4}$ SideA	V- offset $x10^{-4}$ SideB		321A FOR 200°C TEST Serial Number
.05	0	-57	-285	-470		2 - Control
.01	-13	50	181	77		29
.09	-104	-94	58	146		30
.02	-320	-143	231	-7		31
-.01	-237	-10	15	-222		32
-.04	-1769	-220	127	121		33
-.04	-273	-107	-1633	-1943		34
-0.1	-37	-50	7	-17		35
-.03	-142	-125	-112	-233		36
.03	18	-134	375	121		37
.02	-177	-224	-32	-59		38
.04	-260	-160	515	226		39
.01	-155	-140	225	194		40
-.01	45	-37	-266	-165		42
-.01	-94	-42	-7	73		46
.01	-209	-135	647	378		47
.01	-185	-183	-112	-121		48
.01	-345	-152	660	170		49
-.03	-68	128	277	107		50
.004	-150	-99	64	-64		Average
.03	116	91	496	496		Standard Deviation
-0.9	-1.4	-0.4	0.4	0.4		% CHANGE (CONTROL)
5	11000	11000	95000	95000		Typical Value

TABLE V-13a MEASUREMENT DELTAS, PRE AND POST 4000 HR LIFE TEST, @ 25°C; 321A

IDD (mA)	Gain X 10^{-4} SideA	Gain X10^{-4} SideB	V-offset x10^{-4} (V) SideA	V-offset x10^{-4} (V) SideB	Noise (mV) SideA	Noise (mV) SideB	CTE x10^{-6} SideA	CTE x10^{-6} SideB	150°C TEST Serial Number
.07	-2	-24	-93	-116	.02	-0.2	1	2	1 - Control
.14	37	62	-197	-252	.12	.94	0	1	2 - Control
.10	17	19	-145	-184	.07	.46	0.5	1.5	Average
-0.1	-781	-32	172	13	.14	1.10	8	7	4
0.6	-259	-167	750	491	.08	.22	13	10	5
.01	125	109	-326	-344	-0.1	.04	1	2	6
0	-522	-410	1294	1006	-.10	.34	23	22	7
.02	87	139	-293	-392	.02	.47	2	2	10
-.01	-68	17	479	195	.07	.13	8	6	11
0	-473	-217	927	319	-.02	.89	22	13	12
.02	-65	83	343	74	.15	.40	8	5	13
.02	20	187	-13	-161	.13	.15	5	5	15
.09	-469	-178	806	213	-.07	.43	16	9	16
.01	252	690	-611	-639	.15	.20	0	0	18
.01	-139	-36	617	331	0	.13	11	7	20
.04	209	238	-575	-645	.09	.52	1	1	22
-.01	-815	-745	1336	886	.32	.48	31	26	23
0	-1244	-694	1874	959	.14	.48	41	28	25
-.02	-105	-164	69	59	-.01	.64	8	9	26
.04	-526	-301	1527	737	0	.23	19	12	27
.01	-148	-206	-36	-268	.02	.45	9	5	28
.016	-234	-94	463	157	.06	.41	13	9	Average
.03	382	336	734	517	.10	.27	11	8	Stardard Deviation
-1.4	-2.3	-1.0	0.6	0.3	-2	-10	-	-	% CHANGE (CONTROL)
6	11000	11000	100000	100000	.50	.50	999999	999999	Typical Value

TABLE V-13b MEASUREMENT DELTAS, PRE AND POST 4000 HR LIFE TEST, @25°C; 321A

I_{DD} (mA)	Gain x10^{-4} SideA	Gain x10^{-4} SideB	V-Offset x10^{-4} (V) SideA	V-Offset x10^{-4} (V) SideB	Noise (mV) Side A	Noise (mV) SideB	CTE x10^{-6} SideA	CTE x10^{-6} SideB	200°C TEST Serial Number
.07	-2	-24	-93	-116	.02	-.02	1	2	1 - Control
.14	37	62	-197	-252	.12	.94	0	1	2 - Control
.10	17	19	-145	-184	.07	.46	0.5	1.5	Average
-.18	506	565	655	524	.03	-.10	-3	-4	29
-.16	394	656	718	1543	.14	.01	-6	-8	30
-.04	293	961	763	468	.06	.03	-17	-23	31
-.06	373	568	1984	1285	.07	.37	-5	-9	32
- .11	2439	363	1888	1755	.01	.64	1	1	33
-.08	329	380	3433	204	.19	.24	-21	-27	34
-.11	335	158	1406	1038	.01	0	1	1	35
-.04	-297	-100	1699	921	.02	.02	-6	-13	37
-.03	-1464	445	-8931	1415	.02	.47	-3	-3	38
0	167	254	2093	1490	-.11	.15	-4	-7	39
-.13	730	683	1426	1221	-.01	-.02	-8	-10	42
-.18	154	333	1487	1006	-.03	-.53	3	-1	47
-.14	400	431	1679	1437	.05	.32	-1	-3	48
-.01	661	675	992	1205	.08	.80	-6	-6	50
-.09	359	459	806	1108	.04	.18	-5	-8	Average
.06	804	261	2892	450	.07	.33	7	8	Standard Deviation
-3.2	3.1	4.0	1.0	1.3	-6.0	-56	-	-	% CHANGE (CONTROL)
6	11000	11000	100000	100000	.50	.50	999999	999999	Typical Value

The electric field within the depletion region beneath a gate electrode will cause the electrons being transported to gain kinetic energy. If these electrons have sufficient energy to surmount the $Si-SiO_2$ barrier they may be injected into the gate oxide. A fraction of these are trapped which causes a shift in device characteristics. This is a possible cause for the high temperature degradation of transfer efficiency and may also have affected the other parameters. This phenomena increases with temperature and on a transistor also with drain voltage.

The changes seen for the transfer efficiency measurement were quite small and would not be expected to cause any problems in a long term application.

The change in gain on side A of S/N 33 was due to a resistive short between $\phi 1A$ and V_{RA}. This is a layer-to-layer polysilicon short.

The shifts in the remainder of the parameters is due primarily to shifts in the devices due to the high temperature operating stress. Changes in the instrumentation will cause smaller changes than those seen for these life test parts.

Examples of the deltas for specific parts during the course of the life test are given in Table V-14 through V-19. The first three are from the 150 °C group and the second three are from the 200 °C group. The general trends covered above are evident on some of these devices.

Tables V-20 and V-21 contain statistics on each of the parameters measured except for the input leakage current. Table V-20 covers the parameters at +25 °C, -25 °C, and +55 °C at initial characterization. There is a fairly large variation in several of these parameters indicating manufacturing differences. The post-life test statistics are provided in Table V-21. The trends discussed in the above delta analysis are again evident. These measurements were performed at +25°C and cover the 150°C and 200°C life test groups.

The stability of the CCD321A is very good as shown by this high temperature long-term life test.

Assuming an activation energy of 1.0 eV the room temperature operating time to correspond to 4000 hours at 200°C is about 7×10^9 hours.

J. Failure Analysis

The first group of 50 devices tested failed due to bond wire interconnect problems. The gold thermocompression ball bonds lifted from the die surfaces during environmental screen tests. These devices were replaced at no cost by Fairchild. The replacement parts had aluminum wires rather than gold wires.

TABLE V-14 DELTA SHIFTS, 150°C LIFE TEST, S/N 11; CCD321A

T.M	P.E.	GAIN B	GAIN A	V.FF B	V.FF A	N.SE B	N.SE A	CIE B	CIE A
	mA			V	V	mV	mV		
0	5.59	1.179	1.267	9.933	9.754	0.378	0.287	0.999988	0.999982
1D7	5.45	1.149	1.161	1.D1D	9.936				
1D8	5.59	1.147	1.137	1.D42	9.938				
1D9	5.63	1.138	1.172	1.D36	9.955				
1.0	5.51	1.114	1.162	1.D37	9.916				
1.1	5.61	1.139	1.165	1.D54	9.982				
1.2	5.53	1.154	1.164	1.D3D	9.91b				
1.3	5.49	1.109	1.087	9.941	9.855				
1.4	5.44	1.101	1.178	1.D496	9.939				
1.5	5.57	1.179	1.198	9.901	9.874				
1.6	5.51	1.122	1.122	1.D172	9.807				
1.7	5.58	1.101	1.199	9.973	9.825	0.319	0.361	0.999994	0.999990
MEAN	5.55	1.126	1.178	1.D15	9.843	0.448	0.324	0.999992	0.999986
S.D.	0.05	0.023	0.027	0.032	0.057	0.070	0.037	0.000001	0.000004

DELTA SHIFTS

1D7	-0.11	-0.029	-0.054	0.181	0.171				
1D8	0.03	-0.025	-0.089	0.089	0.134				
1D9	0.01	-0.021	-0.047	0.096	0.120				
1.0	0.02	-0.028	-0.043	0.093	0.147				
1.1	0.02	-0.027	-0.017	0.014	0.143				
1.2	-0.05	-0.054	-0.020	0.078	0.171				
1.3	-0.13	-0.010	-0.018	0.043	0.070				
1.4	-0.13	-0.018	-0.027	0.058	0.144				
1.5	-0.02	-0.002	-0.002	0.028	0.027				
1.6	-0.05	-0.074	-0.145	0.034	0.123				
1.7	-0.01	0.017	-0.060	0.019	0.047	0.143	0.074	0.000003	0.000006

TABLE V-15 DELTA SHIFTS, 150°C LIFE TEST, S/N 12; CCD321A

T=N	PD=EA mA	GAIN B	GAIN A	VOFF B V	VOFF A V	NOISE B mV	NOISE A mV	CTE B	CTE A
4	5.83	1.2497	1.2570	±0.0156	9.8723	0.498	0.436	0.999980	0.999965
±07	5.89	1.2034	1.2416	±0.1046	±0.0109				
±08	5.91	1.2013	1.2384	±0.0751	9.9786				
±09	5.84	1.2143	1.2561	±0.0557	9.9496				
±10	5.83	1.2030	1.2403	±0.0703	9.9766				
±11	5.84	1.2031	1.2385	±0.0700	9.9794				
±12	5.89	1.1991	1.2380	±0.0782	9.9801				
±13	5.83	1.2201	1.2616	±0.0539	9.9380				
±14	5.86	1.2056	1.2411	±0.1125	±0.0264				
±15	5.74	1.2066	1.2444	±0.0696	9.9817				
±16	5.74	1.2087	1.2450	±0.0770	9.9794				
±17	5.83	1.2080	1.2597	±0.0475	9.9653	1.192	0.424	0.999992	0.999987
MEAN	5.75	1.2086	1.2476	±0.0674	9.9715	0.745	0.430	0.999986	0.999976
S.D.	0.04	0.0084	0.0136	0.0258	0.0578	0.447	0.006	0.000006	0.000011
		DELTA SHIFTS							
±07	-0.14	-0.0263	-0.0453	0.0690	0.1386				
±08	-0.02	-0.0284	-0.0487	0.0595	0.1063				
±09	-0.01	-0.0154	-0.0510	0.0431	0.0774				
±10	0.00	-0.0267	-0.0467	0.0547	0.1046				
±11	0.01	-0.0266	-0.0487	0.0544	0.1071				
±12	-0.14	-0.0307	-0.0492	0.0606	0.1078				
±13	-0.22	-0.0096	-0.0252	0.0185	0.0657				
±14	-0.25	-0.0239	-0.0460	0.0969	0.1541				
±15	-0.13	-0.0229	-0.0427	0.0542	0.1094				
±16	-0.09	-0.0210	-0.0420	0.0614	0.1271				
±17	-0.00	-0.0217	-0.0474	0.0519	0.0927	0.694	-0.013	0.000012	0.000022

TABLE V-16 DELTA SHIFTS, 150°C LIFE TEST, S/N 13; CCD321A

T.N	POWER MA	GAIN B	GAIN A	VOFF B V	VOFF A V	NOISE B MV	NOISE A MV	CTE B	CTE A
0	5.70	1.1580	1.1637	9.8363	9.8556	0.262	0.306	0.999989	0.999985
107	5.60	1.1175	1.1507	9.9264	9.9033				
108	5.66	1.1137	1.1285	9.9060	9.9501				
109	5.63	1.1232	1.1432	9.8852	9.9284				
110	5.73	1.1167	1.1311	9.9028	9.9553				
111	5.73	1.1194	1.1335	9.8984	9.9509				
112	5.80	1.1176	1.1340	9.8969	9.9462				
113	5.57	1.1381	1.1524	9.8540	9.8985				
114	5.55	1.1277	1.1412	9.9197	9.9741				
115	5.70	1.1429	1.1540	9.8356	9.9066				
116	5.63	1.1410	1.1543	9.8742	9.9287				
117	5.72	1.1463	1.1572	9.8437	9.8899	0.316	0.456	0.999995	0.999993
MEAN	5.69	1.1286	1.1437	9.8833	9.9315	0.439	0.382	0.999992	0.999989
S.D.	0.06	0.0115	0.0116	0.0288	0.0362	0.177	0.076	0.000002	0.000003
		DELTA SHIFTS							
107	-0.04	-0.0205	-0.0330	0.0701	0.1277				
108	-0.03	-0.0243	-0.0352	0.0697	0.1045				
109	-0.07	-0.0148	-0.0205	0.0489	0.0728				
110	0.03	-0.0213	-0.0320	0.0665	0.0997				
111	0.04	-0.0180	-0.0302	0.0621	0.0953				
112	-0.09	-0.0204	-0.0291	0.0607	0.0906				
113	-0.13	0.0001	-0.0113	0.0177	0.0429				
114	-0.15	-0.0103	-0.0225	0.0634	0.1185				
115	0.00	0.0049	-0.0096	0.0193	0.0510				
116	-0.06	0.0036	-0.0094	0.0379	0.0731				
117	0.02	0.0083	-0.0065	0.0074	0.0343	0.354	0.152	0.000006	0.000006

TABLE V-17 DELTA SHIFTS, 200°C LIFE TEST, S/N 30; CCD321A

T.M	PIXEL	GAIN B	GAIN A	VOFF B	VOFF A	NOISE B	NOISE A	CTE B	CTE A
	uV			V	V	uV	uV		
0	5.41	1.2503	1.3171	-0.2526	-0.2013	0.314	0.243	0.999995	0.999987
24	5.21	1.2574	1.3221	-0.2595	-0.2276				
48	5.37	1.2396	1.3216	-0.2413	-0.2011				
72	5.33	1.2945	1.3285	-0.2536	-0.1925				
96	5.29	1.2957	1.3297	-0.2583	-0.1944				
120	5.33	1.3003	1.3311	-0.2223	-0.1652				
144	5.24	1.3255	1.3343	-0.2433	-0.1903				
168	5.15	1.3053	1.3379	-0.2354	-0.2047				
192	5.03	1.3112	1.3404	-0.2555	-0.2283				
216	5.17	1.3132	1.3497	-0.3045	-0.2735				
240	5.14	1.3283	1.3494	-0.3759	-0.2435				
264	5.25	1.3454	1.3555	-0.4059	-0.2731	0.317	0.391	0.999985	0.999985
4848	5.25	1.3053	1.3346	-0.2737	-0.2213	0.315	0.315	0.999983	0.999984
S.D.	0.13	0.0175	0.0118	0.0583	0.0325	0.002	0.075	0.000005	0.000005
		DELTA SHIFTS							
24	-0.20	0.0056	0.0050	0.0159	0.0263				
48	-0.04	0.0098	0.0045	-0.0113	-0.0005				
72	-0.08	0.0135	0.0117	-0.0193	-0.0085				
96	-0.12	0.0159	0.0116	-0.0193	-0.0059				
144	-0.11	0.0192	0.0140	-0.0503	-0.0151				
168	-0.15	0.0248	0.0174	-0.0291	-0.0113				
192	-0.29	0.0245	0.0208	-0.0152	0.0034				
216	-0.35	0.0304	0.0235	0.0529	0.0570				
240	-0.24	0.0574	0.0526	0.0819	0.0772				
264	-0.29	0.0475	0.0323	0.1224	0.0422				
4848	-0.15	0.0556	0.0594	0.1943	0.0715	0.005	0.145	-0.000005	-0.000007

TABLE V-18 DELTA SHIFTS, 200°C LIFE TEST, S/N 31; CCD321A

T_M	PIxEL	GAIN B	GAIN A	VOFF B	VOFF A	NOISE B	NOISE A	CTE B	CTE A
	mV			V	V	mV	mV		
0	3.33	1.0350	1.0487	9.8443	9.8413	0.349	0.355	0.999975	0.999955
2D#	3.33	1.0332	1.0316	9.9515	9.9714				
2D5	3.33	1.0325	1.0251	9.9259	9.9721				
2D#	3.33	1.0382	1.0383	9.9355	9.9476				
2L2	3.33	1.0447	1.0449	9.9337	9.9557				
2L4	3.33	1.1022	1.0356	9.9315	9.9513				
2L2	3.31	1.1111	1.0405	9.8451	9.9455				
2L5	3.32	1.1245	1.0457	9.8523	9.9252				
2L#	3.32	1.1322	1.1021	9.9155	9.9731				
2L5	3.33	1.1458	1.1120	9.9115	9.9383				
2L5	3.33	1.1552	1.1195	9.9295	9.9512				
2L7	3.34	1.1511	1.1280	9.9411	9.9575	0.327	0.330	0.999953	0.999951
PRE	3.33	1.1137	1.0457	9.9122	9.9540	0.352	0.330	0.999954	0.999955
S.D.	0.05	0.0319	0.0154	0.0155	0.0240	0.015	0.025	0.000011	0.000007
		DELTA SHIFTS							
2D1	-0.03	0.0132	-0.0171	0.0372	0.0336				
2D5	0.00	0.0078	-0.0225	0.0315	0.0303				
2D#	0.02	0.0192	-0.0152	0.0122	0.0353				
2L0	-0.01	0.0297	-0.0138	0.0143	0.0354				
2L4	0.01	0.0372	-0.0111	0.0372	0.0335				
2L2	-0.01	0.0451	-0.0082	0.0015	0.0342				
2L5	-0.02	0.0398	-0.0021	-0.0115	0.0339				
2L#	-0.02	0.0372	0.0034	0.0220	0.0315				
2L5	-0.00	0.0305	0.0135	0.0172	0.0225				
2L5	-0.00	0.0212	0.0205	0.0155	0.0397				
2L7	-0.00	0.0351	0.0295	0.0455	0.0755	0.022	-0.054	-0.000022	-0.000014

TABLE V-19 DELTA SHIFTS, 200°C LIFE TEST, S/N 37; CCD321A

T_N	PDwEA mB	GAIN B	GAIN A	VOFF B V	VOFF A V	NOISE B mV	NOISE A mV	CTE B	CTE A
0	3.90	1.1946	1.1769	9.7653	9.4882	0.338	0.342	0.999979	0.999962
007	3.75	1.1799	1.1796	9.8090	9.5116				
008	3.82	1.1767	1.1747	9.8002	9.6101				
009	3.86	1.1924	1.1714	9.7834	9.5910				
010	3.87	1.1797	1.1765	9.7999	9.6125				
011	3.86	1.1785	1.1769	9.7986	9.6166				
012	3.75	1.1757	1.1795	9.8019	9.6120				
013	3.75	1.1966	1.1904	9.7804	9.5865				
014	3.75	1.1775	1.1795	9.8225	9.6446				
015	3.83	1.1914	1.1772	9.8077	9.6273				
016	3.80	1.1965	1.1982	9.8294	9.6464				
017	3.85	1.1946	1.1972	9.8574	9.6581	0.356	0.355	0.999957	0.999956
MEAN	3.82	1.1938	1.1792	9.8051	9.6088	0.348	0.349	0.999973	0.999959
S.D.	0.05	0.0082	0.0170	0.0227	0.0417	0.010	0.007	0.000006	0.000003

DELTA SHIFTS

007	-0.15	-0.0047	-0.0171	0.0437	0.1234				
008	-0.08	-0.0079	-0.0194	0.0340	0.1218				
009	-0.04	-0.0022	-0.0150	0.0241	0.1025				
010	-0.08	-0.0059	-0.0006	0.0345	0.1242				
011	-0.04	-0.0061	-0.0000	0.0335	0.1283				
012	-0.13	-0.0089	-0.0174	0.0366	0.1238				
013	-0.14	-0.0180	-0.0466	0.0150	0.0986				
014	-0.13	-0.0071	-0.0176	0.0366	0.1364				
015	-0.07	-0.0035	-0.0490	0.0424	0.1591				
016	-0.10	-0.0181	-0.0387	0.0641	0.1881				
017	-0.04	-0.0100	-0.0297	0.0921	0.1597	0.020	0.014	-0.000012	-0.000006

Table V-20 Initial Electrical Characterization Parameter Statistics, CCD321A

Parameter	Test Conditions		Spec. Limits Typical[2]	Units	Test Data Summary min.	max.	mean	std. dev.
Device Current	Note 1	-25°C	-	mA	4.71	8.55	6.96	0.98
		+25°C			3.84	7.00	5.69	0.80
		+55°C			3.33	6.01	4.94	0.71
Gain Side A	Note 1 Delta V_{IN} = 0.4 V	-25°C	-	V/V	0.88	1.27	1.13	0.08
		+25°C			0.90	1.36	1.19	0.09
		+55°C			0.89	1.39	1.21	0.10
Gain Side B	Note 1 Delta V_{IN} = 0.4 V	-25°C	-	V/V	0.88	1.27	1.13	0.08
		+25°C			0.90	1.32	1.17	0.09
		+55°C			0.88	1.32	1.17	0.10
Offset Voltage Side A	Note 1 V_{IN} = 5.0 V	-25°C	-	V	8.30	10.10	9.67	0.29
		+25°C			8.45	10.26	9.71	0.31
		+55°C			8.23	10.06	9.46	0.33
Offset Voltage Side B	Note 1 V_{IN} = 5.0 V	-25°C	-	V	8.27	10.08	9.69	0.28
		+25°C			8.42	10.26	9.78	0.29
		+55°C			8.19	10.14	9.58	0.30
Noise Side A	Note 1 V_{IN} = 3.9 V	-25°C	-	mV	0.18	0.99	0.41	0.25
		+25°C			0.21	0.94	0.41	0.19
		+55°C			0.50	2.37	1.04	0.45
Noise Side B	Note 1 V_{IN} = 3.9 V	-25°C	-	mV	0.20	0.99	0.53	0.20
		+25°C			0.21	2.32	0.49	0.34
		+55°C			0.54	3.37	1.38	0.82
Transfer Eff. Side A	Note 1	-25°C	-		..999969	1.0	.999995	.000007
		+25°C			.999934	.999999	.999979	.000018
		+55°C			.999905	.999993	.999965	.000024
Transfer Eff. Side B	Note 1	-25°C	-		.999979	1.0	.999996	.000006
		+25°C			.999949	.999999	.999985	.000013
		+55°C			.999880	.999997	.999973	.000021

Note 1 - V_{DD}=15 V, sampling frequency = 62.5 KHz.
Note 2 - No specifications available.

Table V-21 Parameter Statistics, Post Life Test, CCD321A

Parameter	Test Conditions	Life Test Temp.	Spec. Limits Typical[2]	Units	Test Data Summary min.	max.	mean	std. dev.
Device Current	Note 1	150°C	-	mA	4.00	6.88	5.77	0.64
		200°C			3.84	6.75	5.41	1.07
Gain Side A	Note 1 Delta V_{IN} = 0.4 V	150°C	-	V/V	1.09	1.25	1.17	0.05
		200°C			1.08	1.36	1.21	0.10
Gain Side B	Note 1 Delta V_{IN} = 0.4 V	150°C	-	V/V	0.97	1.26	1.16	0.07
		200°C			1.11	1.35	1.23	0.09
Offset Voltage Side A	Note 1 V_{IN} = 5.0 V	150°C	-	V	9.34	10.05	9.72	0.23
		200°C			9.08	10.36	10.06	0.21
Offset Voltage Side B	Note 1 V_{IN} = 5.0 V	150°C	-	V	9.31	10.06	9.76	0.22
		200°C			9.73	10.41	10.06	0.21
Noise Side A	Note 1 V_{IN} = 3.9 V	150°C	-	mV	0.26	0.55	0.37	0.08
		200°C			0.25	0.51	0.32	0.08
Noise Side B	Note 1 V_{IN} = 3.9 V	150°C	-	mV	0.39	1.42	0.85	0.28
		200°C			0.28	1.02	0.54	0.24
Transfer Eff. Side A	Note 1	150°C	-		.999975	.999999	.999992	.000007
		200°C			.999951	.999991	.999979	.000014
Transfer Eff. Side B	Note 1	150°C	-		.999980	1.0	.999995	.000004
		200°C			.999953	.999992	.999979	.000014

Note1- V_{DD}=15 V, sampling frequency = 62.5 KHz.
Note2- No specifications available.

The second group of parts failed due to dielectric breakdown between the polysilicon layers and between the polysilicon and substrate. The failure analysis report on these devices is given in the appendix since it is not a part of the 4000 hour reliability study. The two parts which are referred to in the Failure Analysis Report which were sent to Fairchild for analysis, were found to have the dielectric layer beneath the poly2 below specification in thickness. This lead to the low level breakdowns.

A third group of 50 parts was supplied by Fairchild at no cost. A summary of the failures which occurred during the course of the test is given in Table V-22. These are discussed in more detail below.

1. CCD321A, Initial Fallout

History: The following parts were removed from test prior to the 4000 hour life test. The times at which each of these exhibited an electricl failure and the nature of the condition are noted below:

Initial Electrical Leakage Measurement

S/N 19	Pin 9	Leakage

Post Initial Electrical Leakage Measurement

S/N 14	Pin 7	Leakage
S/N 24	Pin 9	Leakage
S/N 44	Pin 7	Leakage
S/N 45	Pin 9	Leakage

Post Environmental Screen Test Electricals

S/N 1	Pin 7	Leakage
S/N 17	Pin 7	Leakage
S/N 21	Pin 12	Leakage to Pin 13 and to ground
S/N 43	Pin 12	Leakage to Pin 11

Post 160 hour Burn-in Electricals

S/N 8	Pin 9	Leakage
S/N 9	Pin 4	Leakage to Pin 6
S/N 41	Pin 9	Leakage

Cause: The cause of all of the above failures was electrical breakdown of the dielectric separating the two polysilicon layers.

Conclusion: These failures were due to a weakness in the dielectric between the two polysilicon layers. The electrical and environmental screen tests were adequate in screening out this weakness. Only one additional device developed 1 nA of leakage during the life test.

TABLE V-22 FAILURE SUMMARY, CCD321A

S/N	FAILURE TIME	FAILURE CLASS	EFFECTED PARAMETER	PHYSICAL CAUSE
19	INITIAL ELECTRICAL	CATASTROPHIC	-	LAYER TO LAYER SHORT
14	POST INITIAL ELECT	CATASTROPHIC	-	LAYER TO LAYER SHORT
24	POST INITIAL ELECT	PARAMETRIC	L	LAYER TO LAYER SHORT
44	|	|	L, I, G, V	|
45			L	
1	POST ENVIRON SCREEN	CATASTROPHIC	-	LAYER TO LAYER SHORT
17	POST ENVIRON SCREEN	PARAMETRIC	L	LAYER TO LAYER SHORT
21	POST ENVIRON SCREEN	CATASTROPHIC	-	LAYER TO LAYER SHORT
43	|	|	-	|
8	POST 160 HR 55°C B/I	CATASTROPHIC	-	LAYER TO LAYER SHORT
9	POST 160 HR 55°C B/I	PARAMETRIC	L, G	LAYER TO LAYER SHORT
41	|	|	L	|
49	POST 64 HR/200°C LIFE	CATASTROPHIC	-	IONIC CONTAMINATION
36	POST 256 HR/200°C LIFE	CATASTROPHIC	-	MANUF DEFECT METALLIZATION FAULT
46	POST 256 HR/200°C LIFE	CATASTROPHIC	-	LAYER TO LAYER SHORT
40	POST 500 HR/200°C LIFE	CATASTROPHIC	-	IONIC CONTAMINATION

NOTE: All parametric failures observed were due to layer to layer shorts which may degrade to catastrophic with stress.

Parameter Code: L = Input Leakage Current

I = Supply Current

G = Gain

V = Offset Voltage

Test Method and Disclosure: The pin 7 and pin 9 failures were located in the output section with the leakage being to V_{DD}. Refer to the failure analysis on Fairchild date code 7923 parts. This included serial numbers 14, 24, 44, 45, 1, 17, 8, and 41.

Analysis on serial numbers 9, 21, and 43 is given below.

The leakage related to pins 11, 12, 13, 4 and 6 are in the input section. Pin 11 is ØSB, pin 12 is VRB, pin 13 is VIB, pin 4 is VRA, and pin 6 is $Ø1_A$. ØS and Ø1 are bottom layer polysilicon gates and VR is a top layer polysilicon gate that overlaps them. (See Figure V-59).

S/N 9 was rejected due to a shift in the gain on side A. This was found to be due to leakage between VRA and $Ø_{1A}$. This leakage had the appearance of a leaky reverse breakdown on a junction for both applied polarities. The current leakage was 1-2 microamps at 2 volts. This leads to a modulation of the amount of charge being introduced into the shift register and results in a change in the gain measurements.

S/N 21 was rejected following the environmental screen tests. The transfer function on this part shifted. An input on side B caused a shifted output level. This is similar to the condition on S/N 9. The VRB metallization (pin 12) was mechanically opened and the failure isolated to be between the VRB polysilicon and the Ø1B polysilicon. There was also leakage from these points back to VIB. The input is shown in Figure V-60 with the metallization scribed open.

S/N 43 was rejected following the environmental screen tests. There was again a shift in the input to output transfer function. A leakage path was found between VRB and ØSB. This was 2 uA @ 1.3V one polarity and 1 uA @ 3V the opposite polarity.

All of the above failures are related to dielectric layer breakdowns.

2. CCD321A, S/N 49

History: S/N 49 was removed from the 200 °C group undergoing the 4000 hour life test following 64 hours of operation. Side B on the device went to zero gain and the Voffset value dropped from 9.8 volts down to 4.3 volts.

Cause: The failure was due to contamination on the die surface with the heaviest concentration over the side B output amplifier.

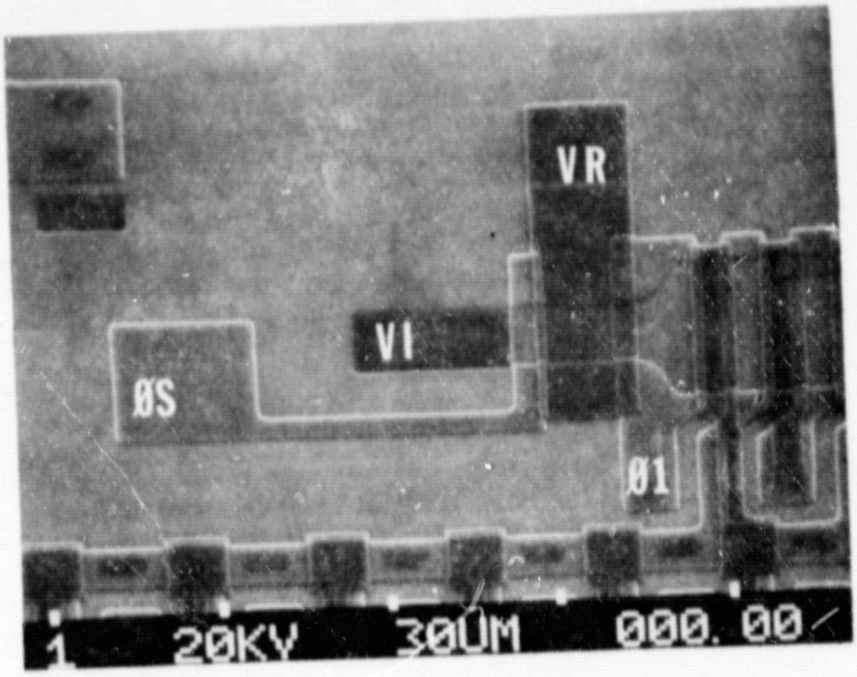


Figure V-59 SEM Micrograph, Input Structure, CCD321A; 800X

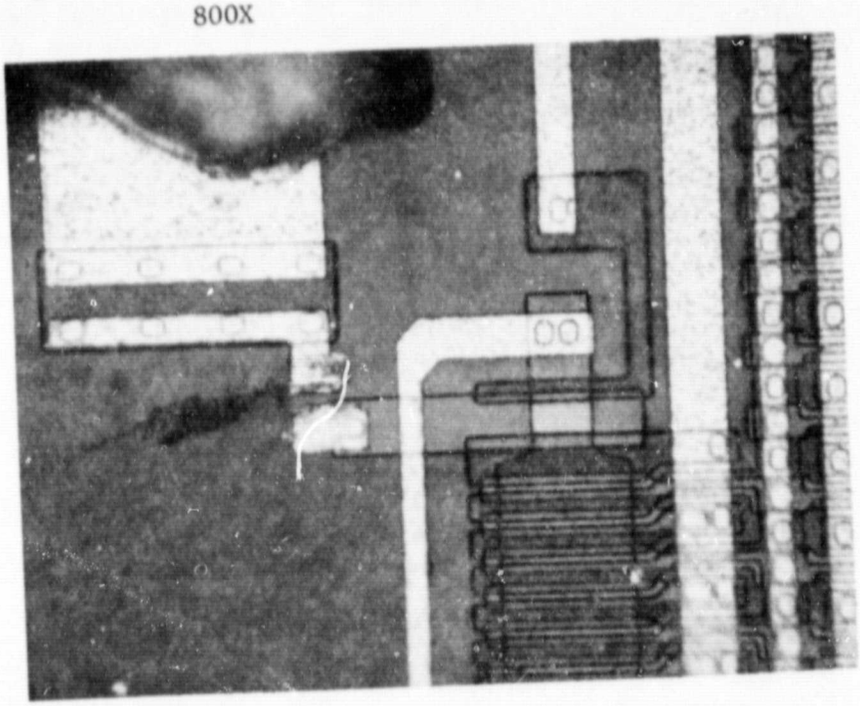


Figure V-60 Input With VR Isolated, CCD321A; 500X

Test Method and Disclosure: The device was electrically characterized and the side A output was found to be operating properly while the side B output stayed at 4.3 volts. The pin to pin measurements found no apparent problems. The package was opened and the contamination was evident Figures V-61 and V-62. The failure was reverified at this point.

The unit was set aside for further analysis and approximately 4 weeks elapsed. Retest at this time found the part to be operating properly with only a slight shift toward a lower voltage output. The offset voltage dropped from 9.8 to 9.1. The gain was back to the original value of 1.1.

This indicates that there was mobile ionic contamination associated with the side B amplifier.

The contamination was analyzed on the SEM and found to be primarily chlorine, potassium, and phosphorous.

3. CCD321A, S/N 36

History: S/N 36 was removed from the 200 °C group following 256 hours of life test. There was no output on the device.

Cause: Failure due to open V_{DD} line.

Conclusion: The appearance of the V_{DD} metallization stripe indicates that there was a masking or etching defect at the point of the open. There was also mechanical damage in this area which may have decreased the metallization corss-sectional area.

Test Method and Disclosure: Electrical measurement found the V_{DD} connection open. The package lid was removed and the open in the metallization stripe was apparent. This was documented on the SEM (Figures V-63 and V-64).

A probe was used to reconnect the metallization stripe by mechanically smearing the aluminum. The part was then retested electrically, however, due to the SEM exposure the unit no longer functioned. Another Fairchild CCD was subjected to the SEM examination and identical electrical characteristics resulted. This is not conclusive but indicates that the only failure on the unit was the open V_{DD} line.

4. CCD321A, S/N 46

History: S/N 46 was removed from the 200 °C group following 256 hours of life test. This part had current leakage associated with pin 9 from the beginning of the testing. Initially this was on the order of 1 uA however it degraded to a short with testing.

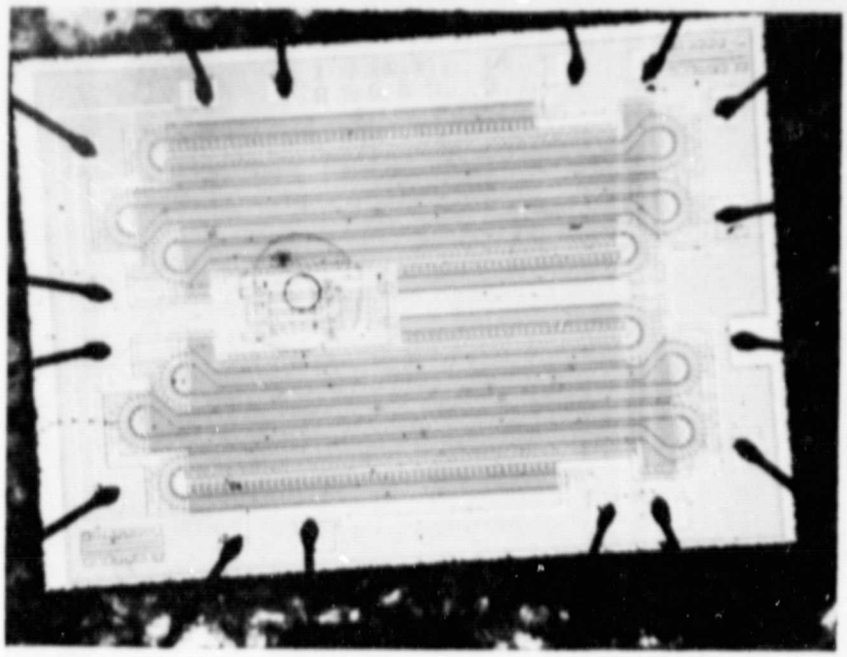


Figure V-61 Die Surface, S/N 49, CCD321A; 40X

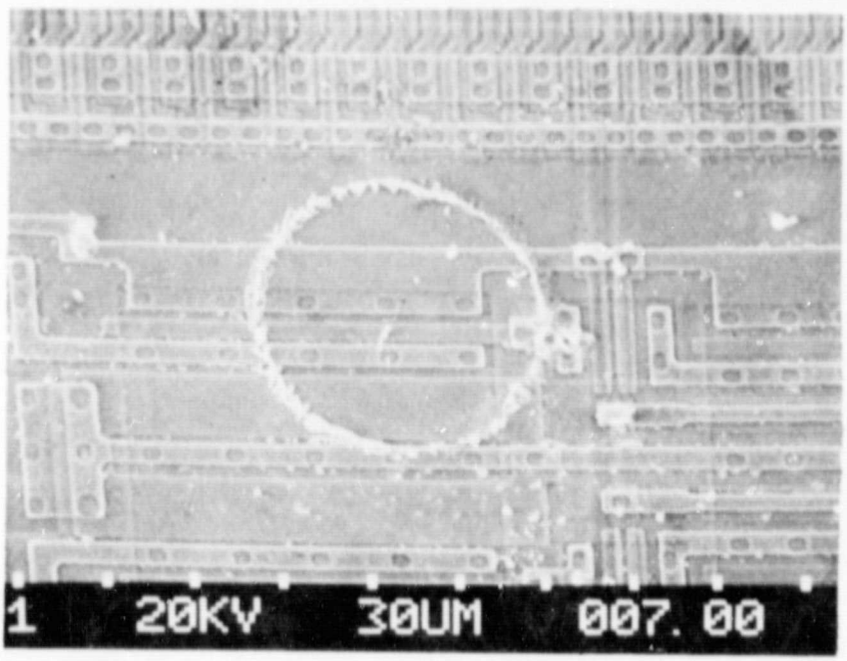


Figure V-62 SEM Micrograph, Contamination on S/N 49, CCD321A; 400X

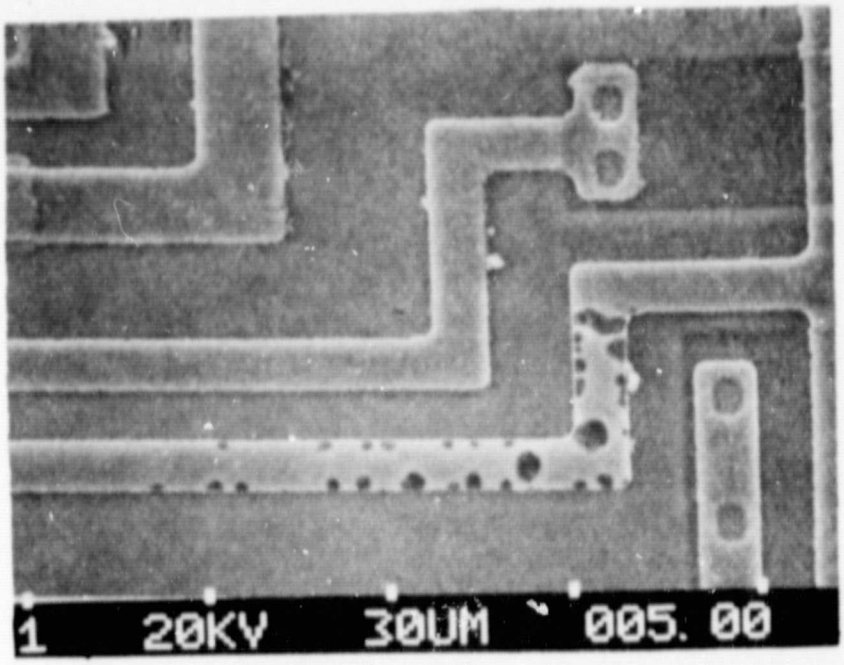


Figure V-63 SEM Micrograph, Open V_{DD} Line, S/N 36, CCD321A; 900X

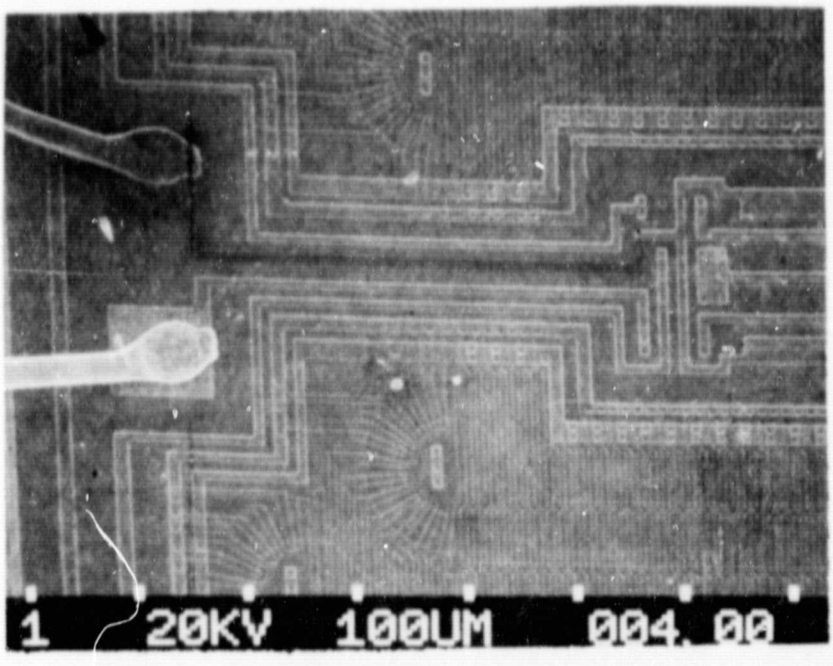


Figure V-64 SEM Micrograph, Voltage Contrast of Open, S/N 36, CCD321A; 150X

Cause: The cause of this failure was a short between the poly1 and poly2 layers. This is identical to other layer to layer shorts analyzed. Refer to 7923 date code failure analysis for detailed discussion of this failure mode.

5. CCD321A, S/N 40

History: S/N 40 was removed from the 200 °C group following 500 hours of life test. The gain on both sides went to zero and the offset voltage dropped from 9.5 volts down to 5.9 volts.

Cause: Cause of the failure was ionic contamination.

Conclusion: Electrical measurement found channelling present on most of the pins. This indicates a surface charge. Following a 10 minute 350 °C bake the part functioned normally.

Test Method and Disclosure: Pin to pin electrical measurement found channelling in the 100 nanoamp range on most pins. The part was opened and examined with no apparent cause for the problem being determined. The unit was then baked at 350 °C for 10 minutes and the part returned to normal electrical readings. The gain was about 1.2 on both sides and the offset voltage was 9.6.

K. Conclusions and Recommendations

This section will address the objectives established for this study and provide a summary of the results.

1. Design Strengths and Weaknesses

The CCD321A-2 has two clocks required for operation. One is the sampling clock and the second is the ø1 shift register transport clock. This is fewer than some 3 and 4 phase systems. The clocks are in the 13 to 15 volt range which makes them more difficult to generate at the higher clock frequencies.

The CCD321A-2 can be used as a single 910 bit delay line or as two separate 455 bit delay lines. With two separate registers it is possible to produce a full-wave output signal if desired.

The transfer function on this device is in the conventional manner with a lower input producing a lower output. This is in contrast to the R5101.

The CCD321A-2 is manufactured utilizing the Buried Channel Charge Coupled Device technology. This provides very good transfer efficiency and high bandwidth.

This device does require several voltage levels to operate, including, a 15 volt V_{DD}, a 5 to 8 volt V_2, a 3 to 7 volt V_{REF}, and a 3 to 7 volt input level.

2. Failure Modes

The prominent failure mode on this part was dielectric breakdown. This can be caused by electrostatic discharge overstress, however, on these parts it was due to an inadequate thickness for the dielectric layer separating the poly1 and poly2 layers. The manufacturer is aware of this problem and it should be solved for future lots.

The other failure mode experienced was contamination of the die surface which created an inversion layer. This was not at an excessively high level and could be eliminated with cleaner processing. One of the two devices which failed due to this would have been rejected if a 100% precap visual had been specified for these parts.

3. Parametric Measurements

For use in a specific application the following electrical parameters should be measured:

a. Input gate leakage - All input gates should be measured for leakage to ground. Leakage between overlapping polysilicon layers in the input, output and shift register circuitry should be measured. All good parts tested were less than 0.1 microamps at 25°C. On a sample basis, parts should be destructively tested to determine if a weak dielectric layer exists. This can be performed by taking all of the inputs on several devices to the input protection diode breakdown.

b. Operating Point - This test verifies that the devices will work over an adequate operating range. This can be performed by monitoring the output waveform resulting from a low frequency sine wave input. The good devices which successfully performed under high stress test passed an initial test of 0.4 volts peak to peak operating around a 3.7 volt d.c. input. (VR = 5.0 volts.)

c. Gain - This parameter should be measured in conjunction with the operating point. It is recommended that a minimum value of 0.7 be used with an input per para. b above. This is about 5.4 standard deviations above the mean values in Table V-20, thus indicating the probability of rejecting a good part is very low, less than .00001%.

d. Bandwidth - The bandwidth on these devices has been excellent, limited only by the clocking rate. This should be measured or the parts should be measured at the frequency at which they are to work to verify the performance of each lot. The manufacturer's specification of 4.5 MHz can be utilized, however, from this study a bandwidth equal to one half of the clock frequency is practical.

e. Device Current - From Table V-20 it is recommended that this value be specified at 9 mA at 25 °C under the test conditions specified therein. This value is about 4.1 standard deviations from the mean value of 5.69 mA, thus indicating the probability of rejecting a good part is less than .002%.

4. Burn-in Circuit

The burn-in circuit utilized for this study provides dynamic operation of these circuits. The voltage levels utilized provide adequate stress to properly determine the reliability of the parts in a burn-in test.

5. Changes to Upgrade Reliability

The oxide thickness and quality needs to be carefully controlled and monitored during the manufacturing process. Since the dielectric layers which failed were in the input and output circuits the use of these dielectric layers for a mask during the n+ diffusion needs to be evaluated.

These circuits are very temperature sensitive and the manufacturers limits of -25 °C to +55 °C are reliable limits when parts are screened as recommended herein. These limitations are inherent in the device themselves. However, these parts are not damaged by operation up to 125 °C and above. Additional characterization to determine performance parameters and operating limitations at higher temperatures will yield data which may be useful in specific applications.

6. Screening Recommendations

The electrical screening should be as discussed in the parametric section. Environmental screening was performed per MIL-STD-883, Method 5004. The results of the life test indicates that this was adequate to provide reliable devices. The 160 hour burn-in was performed at 55 °C. This is the maximum operating temperature as specified in the manufacturers' data sheet. The results of this study indicate that this can be raised to the 125°C level specified in Method 1015.

7. Application and Derating Guidelines

The CCD321A-2 is an analog shift register intended for video signal-delay applications. Some of these applications were discussed in the introduction. New applications are being developed as the technology progresses.

There was no evidence that device derating is required. The device as used with an emitter follower output will operate at the levels specified in the data sheet.

8. Degradation of Charge Transfer Efficiency with High Temperature Operation.

Transfer efficiency was seen to decrease slightly for the 200°C life test group. This type of change can occur if there is an increase in the silicon defect density, an increase in fixed charge loss or a change in the charge density within the oxide. This latter effect can be due to hot electron injection as discussed in the data analysis section.

The electric field within the depletion region beneath the gate electrodes will cause the electrons being transported to gain kinetic energy. If these electrons have sufficient energy to surmount the silicon-silicon dioxide barrier they may be injected into the gate oxide. A fraction of these are trapped which causes a shift in device characteristics. This phenomena has likely contributed to the shifts seen. It is important to note the acceleration factor related to high temperature operation. Assuming an activation energy of 1.0 eV, 1 hour at 200°C is equal to 2 million hours at 25°C. The device shifts with 4000 hours at 200°C are therefore very small for the amount of stress.

VI. Appendix

1. CCD321A Failure Analysis Report

2. R5101 Data Sheet

3. CCD321A Data Sheet

MARTIN MARIETTA

FAILURE ANALYSIS REPORT

Form DEN 354580(11-69)

REPORT NUMBER	
C90116	
DATE	PAGE
04 Dec 1979	1 of 14

MANUFACTURER	ANALYSIS FACILITY	FAILURE LOCATION	LOT NO.	SERIAL NO.	CODE DATE
Fairchild	MMC/F/A Lab	RDL	-	Noted	7923

PART NUMBER	PROJECT/VEHICLE NO.	FAIL. DATE	PART NAME
CCD 321A	DCCD	10/29/79	CCD

This report presents the (1) History, (2) Cause, (3) Conclusion, (4) Test Equipment Utilized, (5) Test Method and Disclosure

HISTORY

Three CCD's were selected for failure analysis. The history of each is given here:

S/N 2 passed initial electrical testing at room temperature. The next test was the same electricals at +55°C. S/N 2 failed at this time and electrical testing found pins 6,7, 9 and 10 to be excessively leaky. The current measured 11μA, 18μA, 73μA, and 1μA respectively.

S/N 43 passed the testing at which S/N 2 failed, and also bandwidth testing at +25°C, -25°C and +55°C. It then passed leakage current testing at +25°C but failed when the temperature was raised to +55°C. Pin 7 measured 100μA and pin 9 measured 2μA.

S/N 7 passed all initial electrical characterization. It then went through an environmental screen test including, 24 hours of stabilization bake at 150°C, 10 temperature cycles from -65°C to +150°C, constant acceleration at 30,000 g and fine and gross leak testing. Electrical testing at this time found side A to be nonfunctional and both pin 7 (side A) and pin 9 (side B) to be leaky. Pin 7 measured 26μA and pin 9 measured 0.1μA.

In addition to these three devices, 2 parts were returned to Fairchild for their analysis.

CAUSE

The cause of the failures was a breakdown of the dielectric isolating the polysilicon layers from each other and/or the polysilicon from the silicon.

CONCLUSION

The test equipment utilized to excerise these CCD's had been used previously with

ORIGINATOR	TITLE	DISTRIBUTION
D. Wilson	Senior Engineer	

CORRECTIVE ACTION & RECOMMENDED DISPOSITION

CORRECTIVE ACTION ENGINEER

APPROVAL	ORIGINATING GROUP TITLE	APPROVAL	PRODUCT INTEGRITY ENGINEER
	T.M. Wilson, Lead Engineer, F/A Lab		
	SOURCE QUALITY		MISSION SUCCESS/MISSION ASSURANCE

CONCLUSION CONT'D

50 other parts of the same type with no failures occurring. The equipment was also carefully checked following these failures to verify that no spiking or other electrical stress was being applied to the parts. Handling precautions were observed due to the electrostatic sensitivity of these devices. It is not believed that the parts received any abnormal electrical stress.

All of the failures analyzed were isolated to the output amplifier section on the CCD. The leakage currents seen on all of the devices are shown in Table I. Note: 1 volt =10 microamps. Pins 7 and 9 are the most common leakage path. The structure associated with these pins is shown in photos 1 and 2. There are two polysilicon layers. The top layer is connected to pin 7 or 9 and the bottom polysilicon layer is connected to VDD (pin 16). The appearance of this area on S/N 43 is shown in photos 3 and 4. The other area found to be shorted is shown in photos 5 and 6. This is the gate of the MOSFET identified as Q1 and Q9 in Figure 2. The external connection to this point also goes to numerous other polysilicon gates along the channel, however, only the gate in the output section experienced a failure.

It appears that there is a weakness associated with the dielectric in the output section of this CCD. The polysilicon in this area is used as the mask for the source and drain diffusions. It is not understood at this time how the diffusion process can degrade the dielectric strength. Consultation with Fairchild will continue until the cause of the failures can be better understood.

TEST EQUIPMENT UTILIZED

Tektronix 576 Curve Tracer	EQ529108
Zeiss Stereomicroscope	EQ526435
Zeiss Universal M Microscope	EQ527339
Cambridge S-180 SEM	EQ534953
Micromanipulator Probing Station	S/N 795812

TEST METHOD & DISCLOSURE

Pin-to-pin electrical characterization was performed on a good device and on serial numbers 2,7, and 43. VGG, VSS, and VDD were measured to each of the other pins.

The packages were then carefully opened by mechanically grinding the lid until it was very thin and then peeling it back to expose the die cavity. Visual examination found two anomalies however, these were not associated with the failures. S/N 2 had a silicon particle on the surface which was present during the manufacturing process (photo 7). The aluminum metallization is seen to be delineated over the top of the particle. S/N 7 had a metallization stripe connected to pin 4 which had been mechanically scraped (photo 8). There was adequate metal to provide electrical continuity, however, failure may have occurred at this point with time.

The first device analyzed was serial number 43 since its failures were the most severe. Pins 7 and 9 were shorted to VDD. The shorts were isolated by mechanically scribing open the metallization stripes as shown in photo 9. This isolated the failures to one side of the overlapping polysilicon structure. By chemically removing the oxide over this polysilicon structure the sites of the failures were visible (photo 3 and 4). These type of appearances have been seen previously on Fairchild devices but never fully explained. Copies of these photographs were sent to Fairchild for their comments.

TEST METHOD & DISCLOSURE CONT'D

S/N 7 had leakage associated with pins 7 and 9. With pin 7 positive and VDD negative the leakage was 10 microamps at 11 volts. With pin 7 negative and VDD positive the leakage was 10 microamps at 14 volts. Pin 9 measured 10 microamps at 16 volts both polarities. These were once again isolated to the overlapping polysilicon structure. The electrical characteristic of these two leakage paths were documented with the sites isolated (photo 10 and 11). Chemical stripping and careful examination on the SEM could not locate a failure site.

S/N 2 had leakage associated with pins 6,7,9 and 10. The leakage on pin 9 was once again isolated to the overlapping polysilicon structure. The leakage on pin 7 disappeared before it could be isolated. The leakage on pins 6 and 10 was more difficult to isolate due to the large number of polysilicon gates to which these pins connect. By stripping the metallization, a current was forced through the polysilicon layer and the voltage drop along it was measured. The location of the short was then isolated to a small portion of the polysilicon. An ultrasonic cutter was then used to open the polysilicon as shown in photo 12. This isolated the leakage path to the polysilicon gate of transistor Q1. This area and that area on transistor Q9 were documented on the SEM (photos 13 and 14). These areas were chemically stripped and the failures sites seen. They appeared to be small holes in the dielectric which were dilated by current flow (photos 15 and 16).

TABLE I POST SCREEN LEAKAGE MEASUREMENTS

S/N	Pin	Voltage Reading	S/N	Pin	Voltage Reading	S/N	Pin	Voltage Reading
4	7	.009	28	7	.029	48	7	10.8
	9	.029		9	3.96		9	9.97
7	7	2.61	29	11	.506	49	4	.0002
	9	.014		12	.058		5	.059
9	7	.024	30	7	10.9		9	.064
	9	.038		9	.015			
10	7	.169	31	7	.050			
11	6	.540		9	.500			
	7	.037	33	7	.015			
	9	10.7		9	.019			
	10	.002	36	7	1.78			
	11	.195		9	10.4			
	12	.005	37	7	.014			
13	7	2.74		9	3.82			
	9	1.50	38	9	.045			
	11	.206	39	7	.010			
15	7	4.23		9	.034			
	9	.027	41	6	6.98			
17	7	.840		7	.003			
	9	9.74		9	.069			
18	9	.3000		10	.429			
20	9	.260	42	9	.155			
21	7	10.9	44	7	10.8			
22	7	.034		9	10.8			
	9	2.51	45	4	.980			
23	7	10.2		5	.188			
24	7	.142		7	.009			
	9	.040		9	4.57			
25	7	10.3	47	7	10.8			
27	7	3.49		9	.007			
	9	.094						

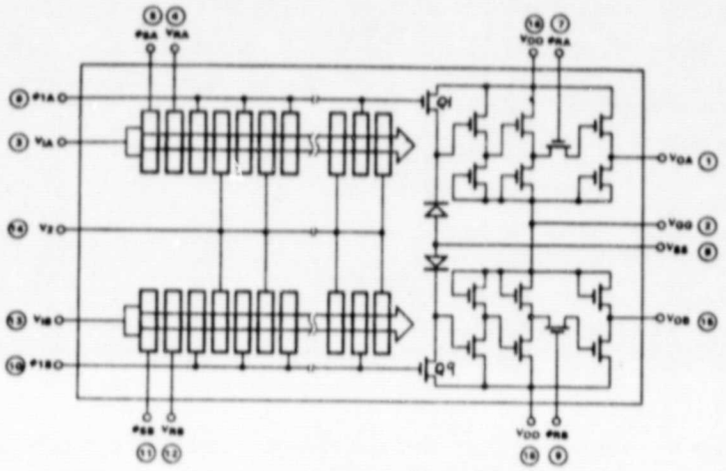


Figure 1 Package Pinout

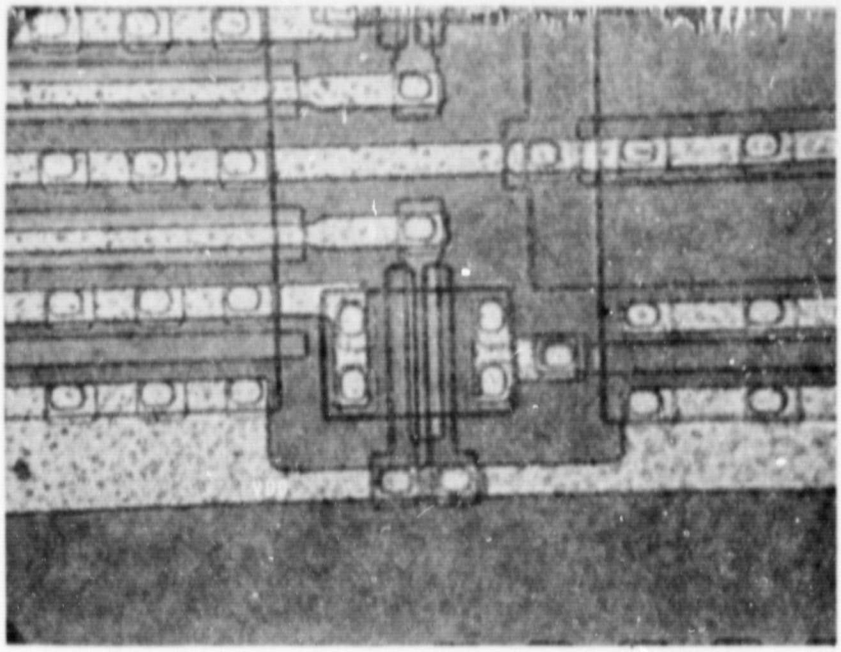


Photo 1 Overlapping polysilicon structure with pin 9 and V_{DD} marked: 500X.

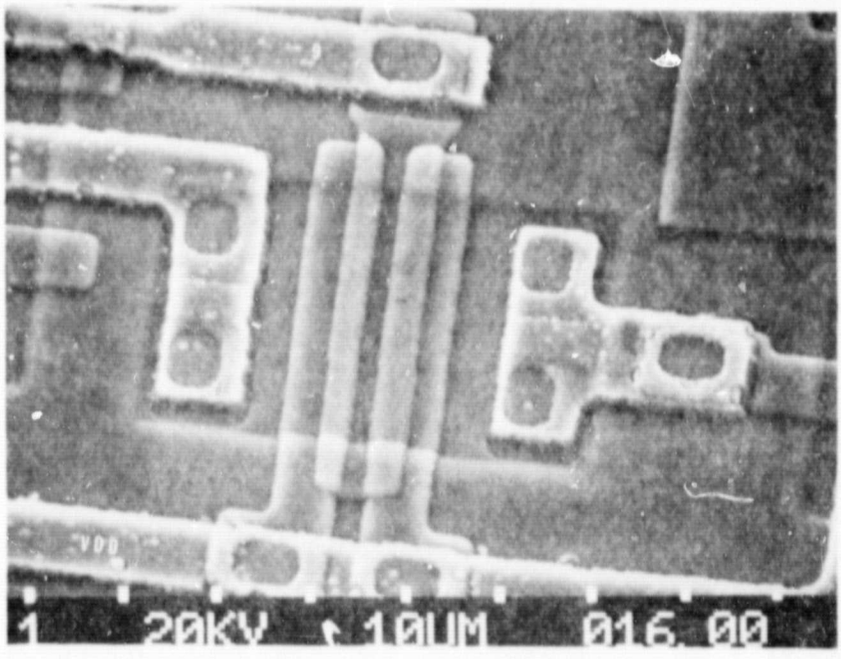


Photo 2 SEM micrograph, same area as photo 1: 1300X.

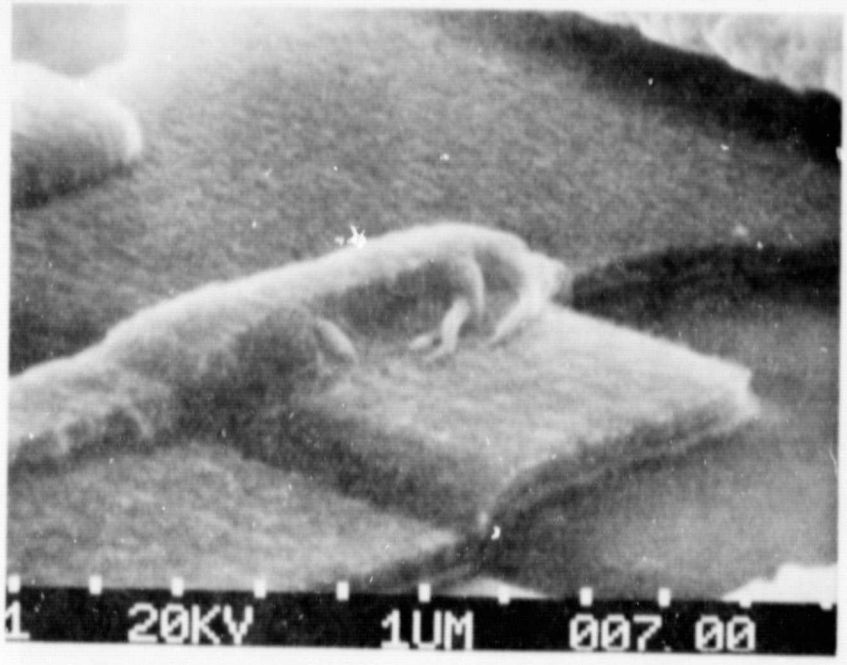


Photo 3 SEM micrograph, ØRA polysilicon to polysilicon short: 11,000X.

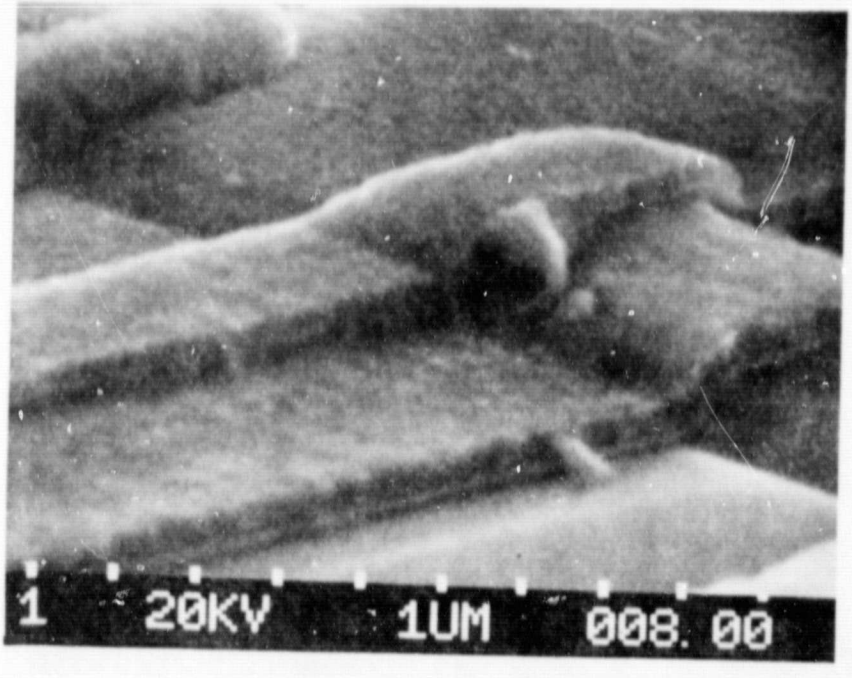


Photo 4 SEM micrograph, ØRB polysilicon to polysilicon short: 11,500X.

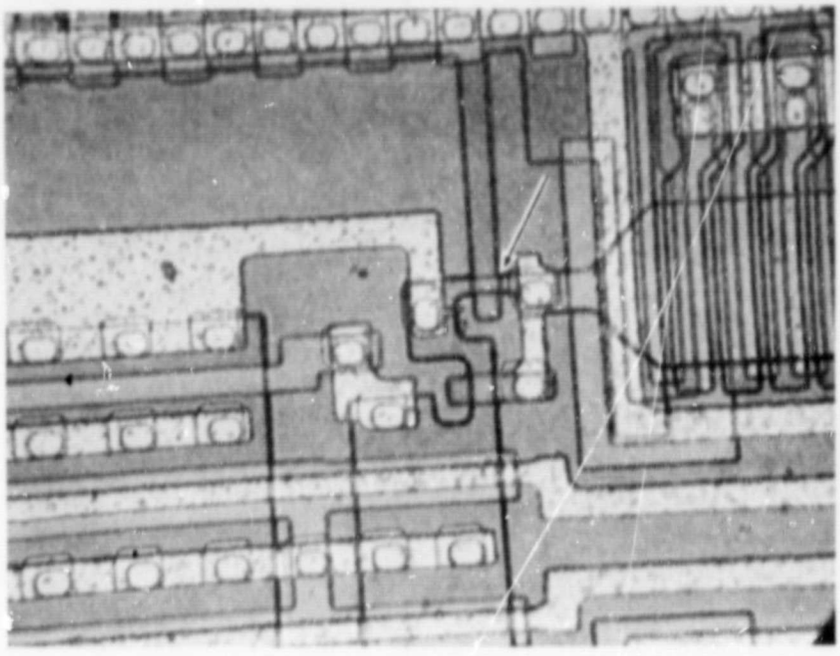


Photo 5 Q_9 gate shown at arrow: 500X.

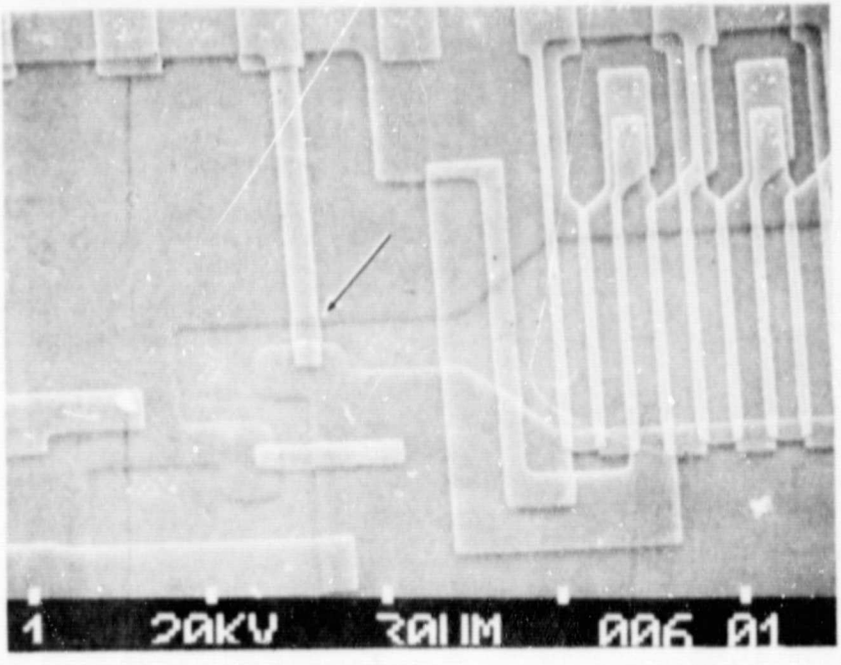


Photo 6 SEM micrograph, same area as ,hoto 5 with metallization stripped: 800X.

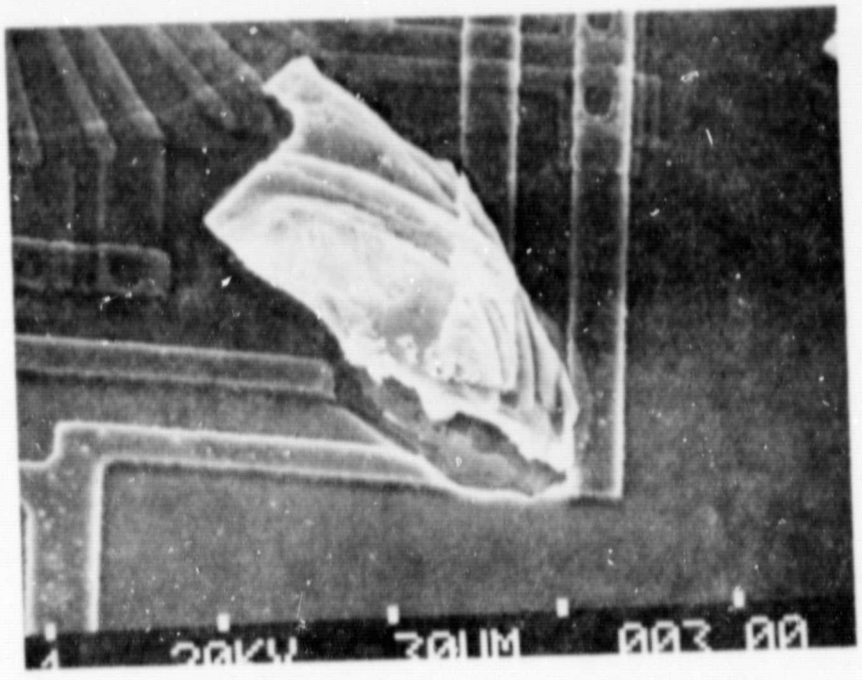


Photo 7 SEM micrograph, silicon particle on S/N 2: 1000X.

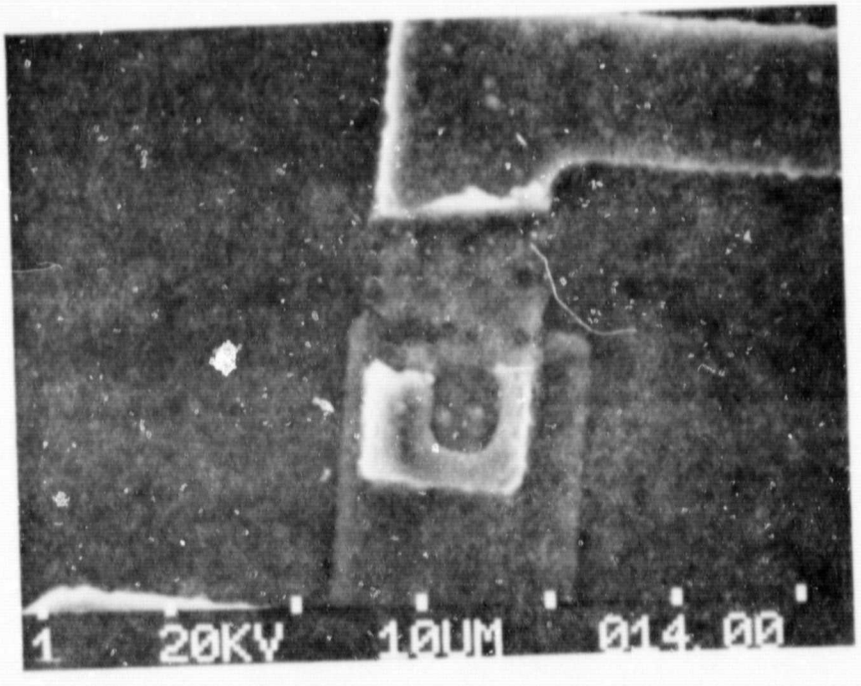


Photo 8 SEM micrograph, scraped metallization on S/N 7: 2100X.

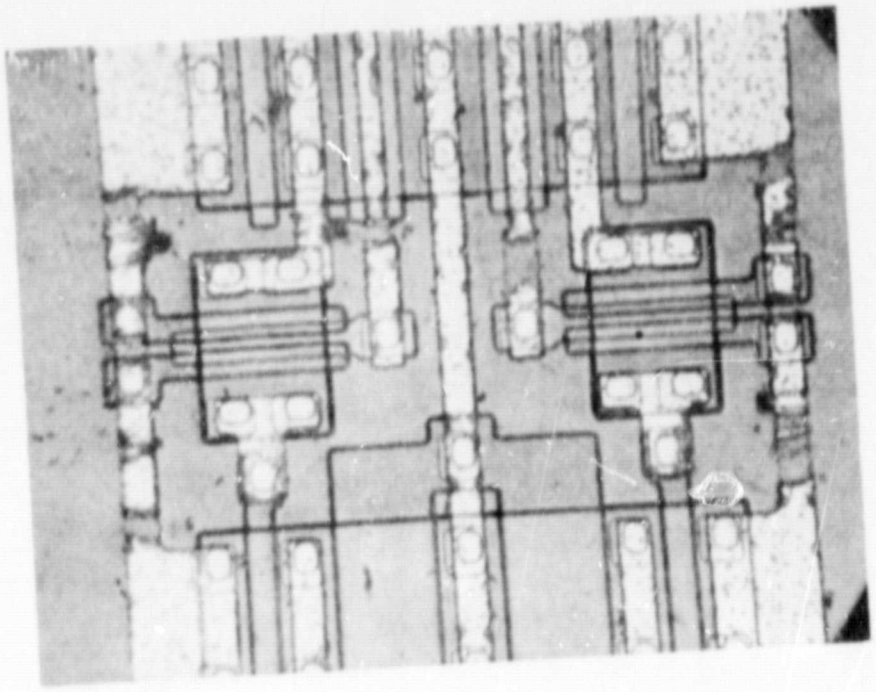


Photo 9 Mechanical isolation of failure on overlapping polysilicon structure of ØRA and ØRB: 500X.

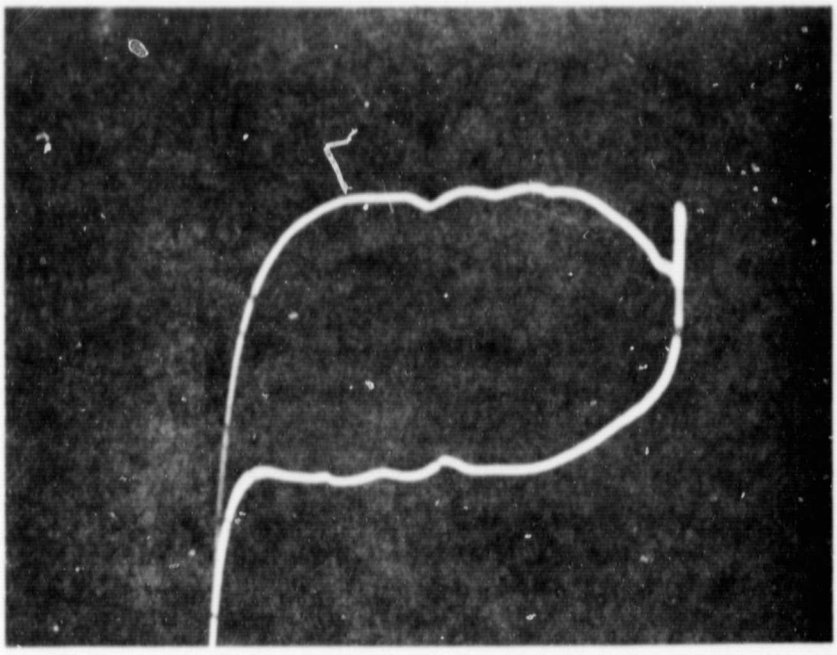


Photo 10 Pin 7 to V_{DD}, 5 volts/horizontal division; 2 microamps/vertical division.

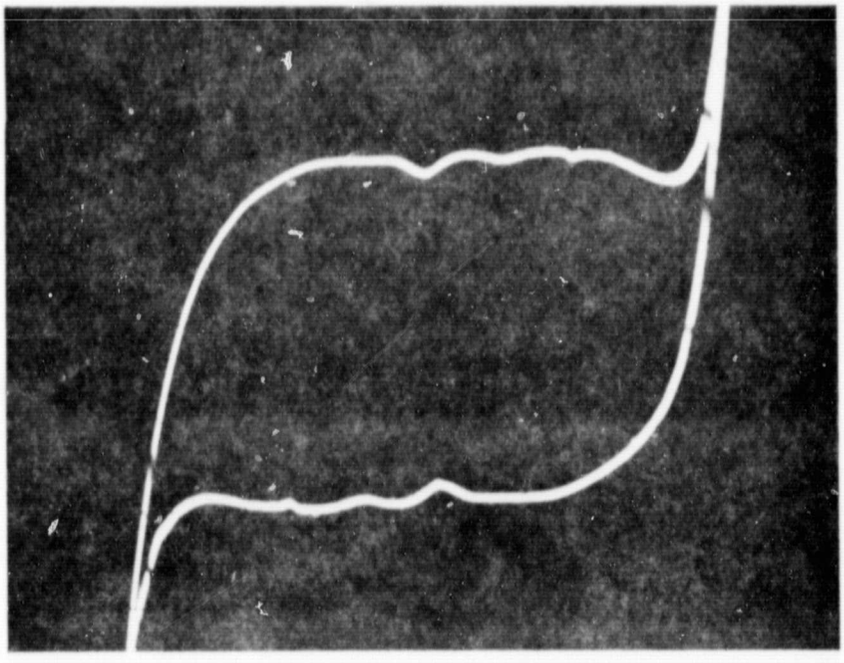


Photo 11 Pin 9 to V_{DD}, same scale as photo 10

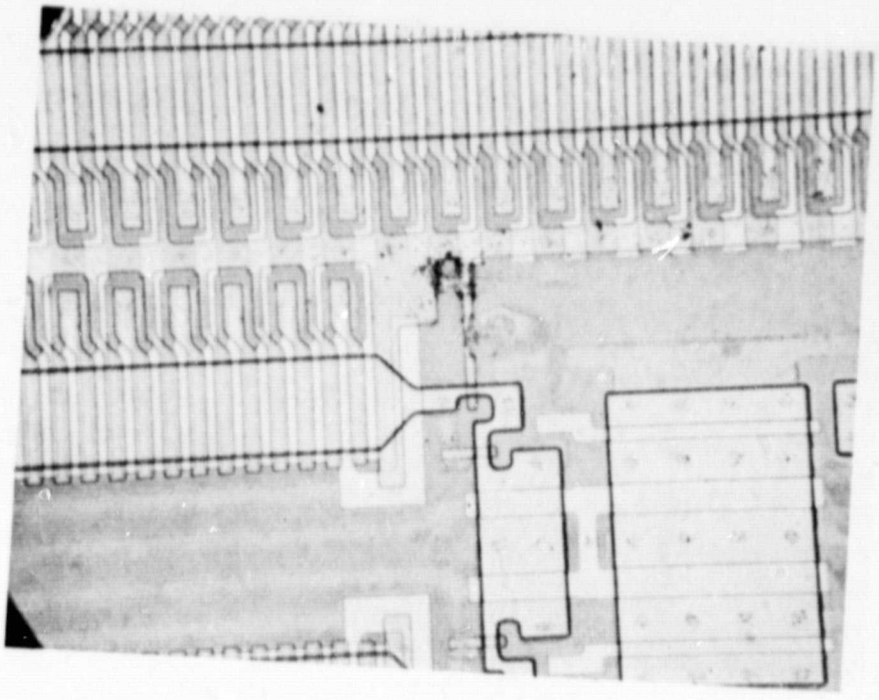


Photo 12 Isolation of Q_1 gate using ultrasonic cutter; 300X.

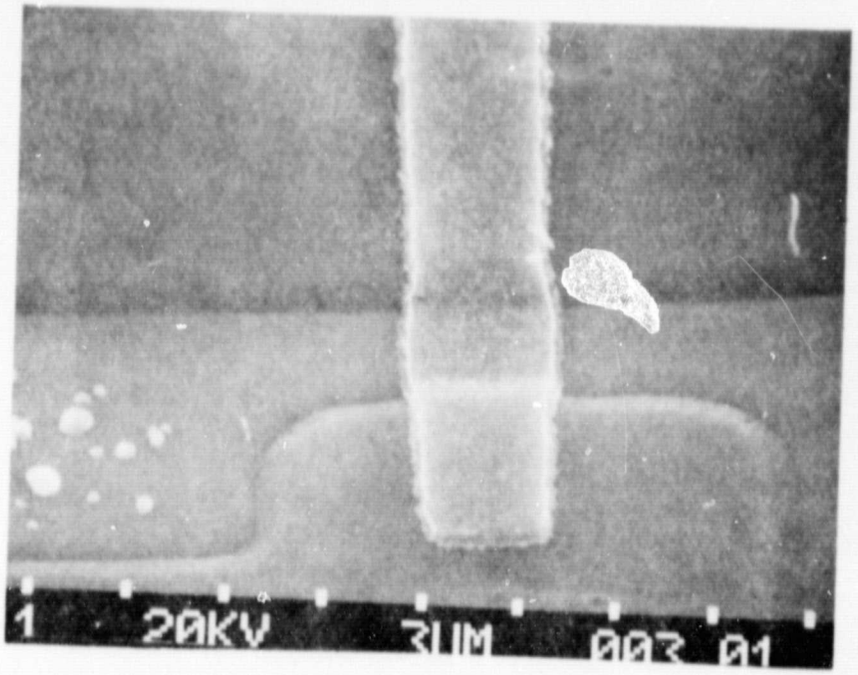


Photo 13 SEM micrograph, transistor Q_1 gate: 4500X.

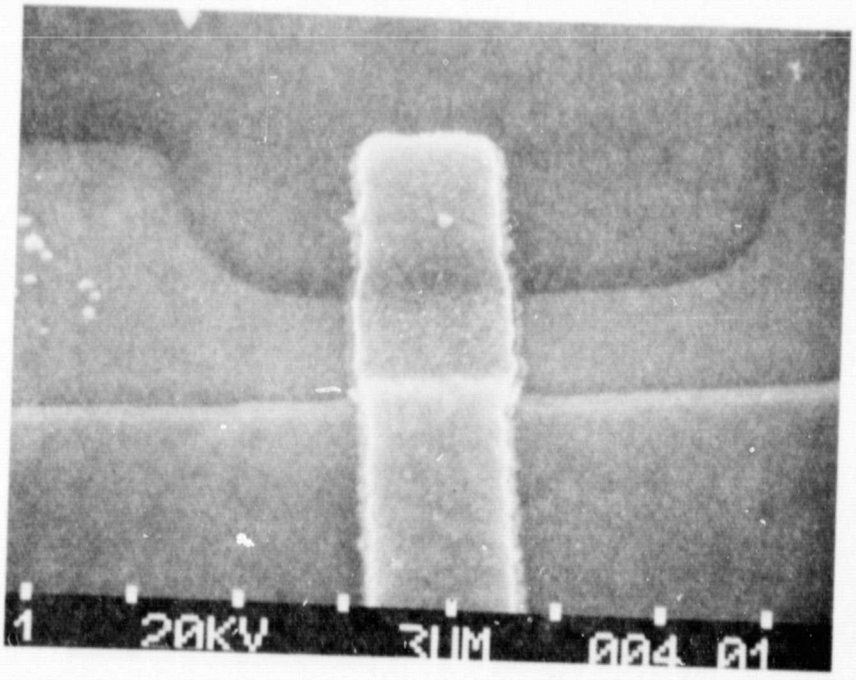


Photo 14 SEM micrograph, transistor Q_9 gate: 4500X.

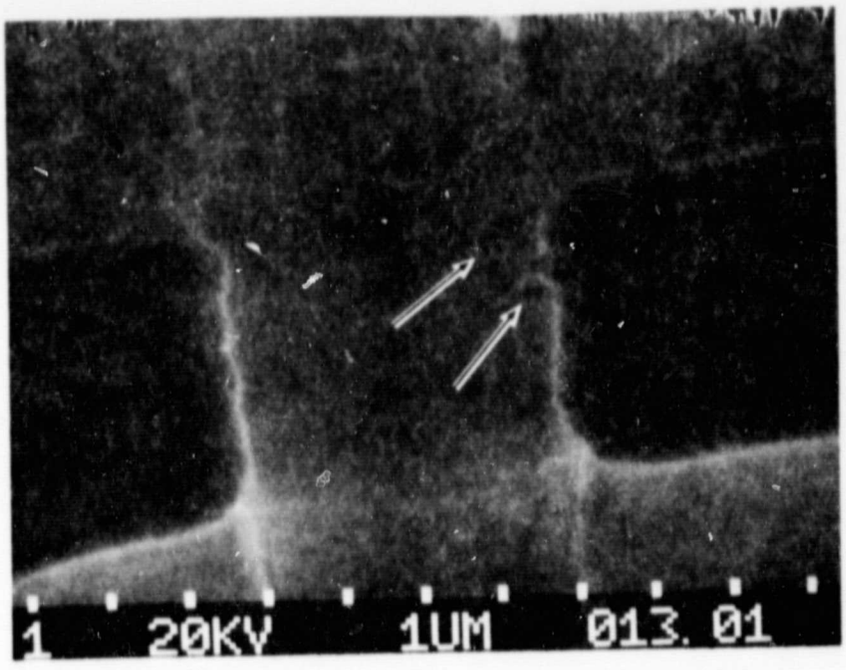


Photo 15 SEM micrograph, transistor Q_1 with arrows indicating failure sites: 10,000X.

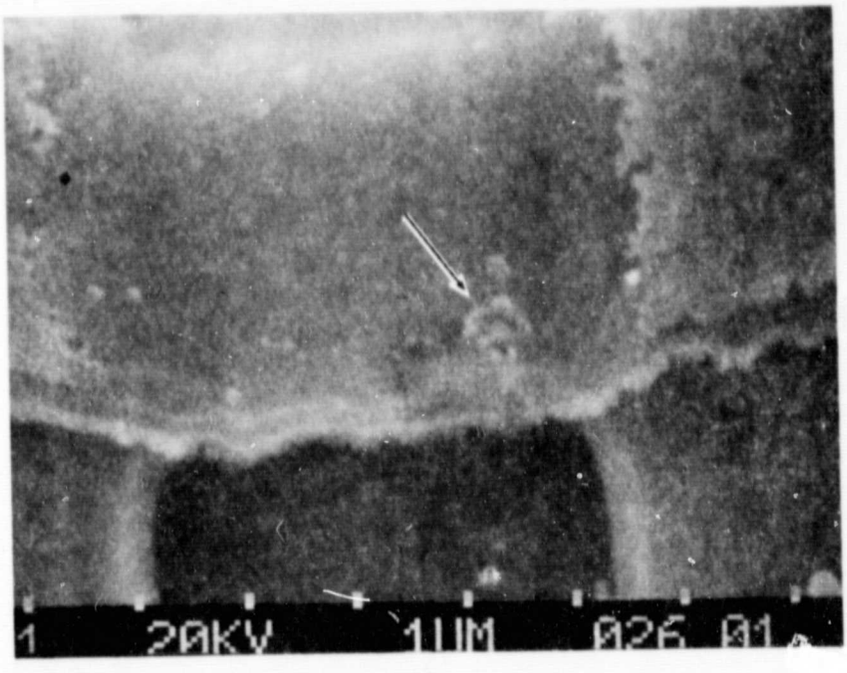


Photo 16 Sem micrograph, transistor Q_9 with arrow indicating failure site: 15,000X.

NTRODUCTION

he R5101 is a monolithic four-phase *C*harge *C*oupled *D*evice CCD) which provides first-in-first-out storage for 2000 quential samples of an analog input signal. It is intended or audio signal-delay applications and is self-contained with n internal four-phase clock generator-driver combination which can be slaved for serial operation. The R5101 is available in a 22 pin dip package with connections as shown in Fig. 1.

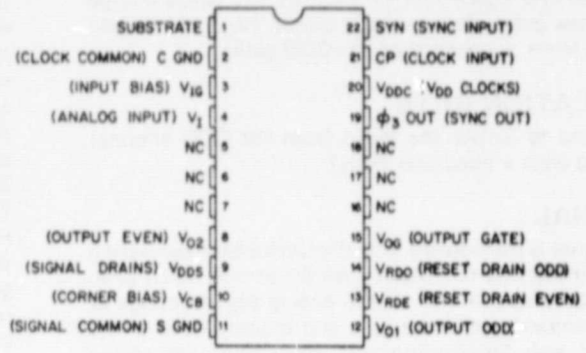


Figure 1. R5101 2000-Sample Delay Pin Configuration.

EY FEATURES

- **2000 samples of audio delay in a single DIP**
- **On-chip driver requiring only single phase 5V clock.**
- **Charge-Coupled Device technology**
- **Wide dynamic range S/N > 70 dB**
- **Clock-controlled variable delay**
- **Sample rates from 4 KHz to 2 MHz**
- **Delays from 1 msec to .5 sec**
- **On-chip output circuit provides full-wave output**

TYPICAL APPLICATIONS

- **Reverberation effects in stero equipment**
- **Sound effects for musical instruments**
- **Data buffering**
- **Variable speech control – pitch correction**

ENERAL DESCRIPTION

ie Reticon R5101 is a self-contained monolithic charge-upled delay device which consists of a charge-transfer annel controlled by a series of gates driven from an on-chip ur-phase driver. The four-phase clocks drive four arrays of quential gates which form potential wells in the channel neath them. The signal is sampled at the rate of one-half the input clock frequency and these wells carry the arges (which represent samples of the input signal) sequenlly through the device, advancing one stage for each two ut clock periods. Figure 2 shows a simplified schematic gram of the device.

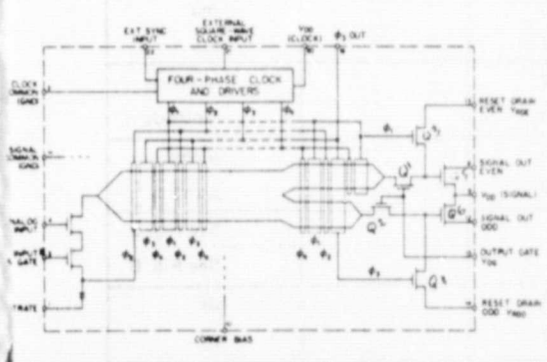
though there is only one delay line, two outputs are proed, labeled odd and even signal outputs. At the output d of the device, the signal is divided into two paths, one ssessing an extra one-half sample time of delay. The extra ayed output is labeled the even signal out and the other nal, taken from the 2000th stage, is labeled odd. This tput arrangement as shown in Fig. 2 gives the user the tion of multiplexing the two outputs through a simple der circuit to obtain a single full-wave output.

gure 3 shows the timing relationship of the signal outputs ative to the external clock input. Two of the internally generated four-phase clocks are also shown. Since $\emptyset_3$ is complement to $\emptyset_1$ and $\emptyset_4$ is complement to $\emptyset_2$, only $\emptyset_3$ and $\emptyset_2$ are shown.

OUTPUT SIGNAL

The output signals as seen in Fig. 3 are produced through a gated charge amplifier during the alternate low-level portions of $\emptyset_1$ and $\emptyset_3$. The odd sampled signal is produced at the output of the odd source follower when the odd reset FET is opened by $\emptyset_3$ going low, then when $\emptyset_3$ rises it resets the gate node of the odd source follower. Simultaneously with the rise of $\emptyset_3$, $\emptyset_1$ falls and the even reset FET's gate is pulled low thereby producing a signal at the output of the even source follower. On the next following half clock cycle this source follower node is reset and the cyclic pattern is repeated while producing a sequence of negative going pulses with the sampled signal super-positioned on the low half cycle as shown in Fig. 3.

The reset level is determined by the reset voltage applied to the reset FET drains. These inputs are seen in Fig. 2.



re 2. Equivalent Circuit for R5101 2000-Sample Delay.

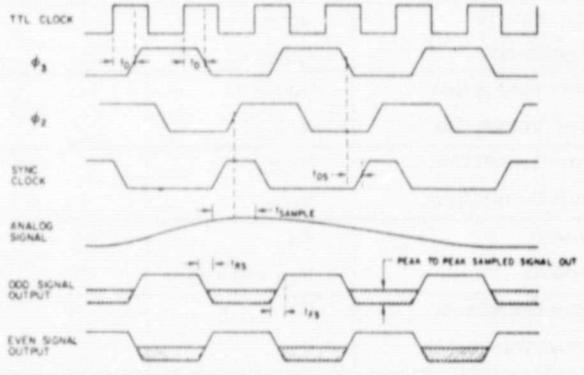


Figure 3. R5101 Relative Timing Diagram.

ETICON CORPORATION 910 Benicia Avenue, Sunnyvale, California 94086
hone: (408) RET-ICON, (408) 738-4266, TWX: 910-339-9343

OUTPUT ISOLATION GATE

In additon to the reset and source follower FETs there is a control FET in the signal line of each of the gated charge amplifiers. These gates are externally biased (V_{OG}) to isolate the reset node from the output of the CCD gates.

INPUT ISOLATION GATE

This gate is used to isolate the input from the CCD channel and is operated with a fixed bias (V_{IG}).

INPUT SIGNAL

The analog signal is introduced into the device by modulating the quiescent input bias condition with the analog input gate. A signal charge proportional to the analog signal voltage at the gate is accepted under the gate and is sampled into the CCD potential well terminating with the rising edge of the $\emptyset_2$ clock cycle, thus locking the analog data into the CCD on the rising edge.

Another function served by the input gate is the adjustment of the input bias V_I. Nominally this gate operates with ≅ 4.5 volts dc bias; however, ±2volt adjustment should be provided to allow for variations in the optimum bias for each device. This arrangement is normally achieved by coupling capacitively into the input and providing bias through a 100 KΩ isolation resistor, using a potentiometer to vary the bias potential over the desired range.

THE CLOCK AND DRIVER

The four-phase clock is generated by driving an internal J-K flip-flop from an external *square-wave* clock with non-critical amplitude of from 5 volts to V_{DD}. The output of the internal flip-flop is isolated from the clock lines by means of buffer drivers. Timing for the flip-flop is controlled by each transition of the input clock, so this latter must be a square wave, as generated by the circuit of Fig. 9.

SYNCHRONOUS OPERATION OF MULTIPLE DEVICES

In order to ensure synchronization between multiple devices, either in a serial or parallel configuration, the internal flip-flops of the on-chip clock drivers must be in phase. In order to easily accomplish this, the $\emptyset_3$ clock (see Fig. 5) is brought as an output to Pin 19 and this signal can be used to generate the synchronization pulse. The requirement for the SYNC pulse is that it be high during the time that $\emptyset_3$ is low (Figure 3). A possible circuit to generate the SYNC pulse is shown in Figure 4 in which the $\emptyset_3$ output is used as an input to a dual monostable. The first monostable generates a delay to assure that the pulse will occur while $\emptyset_3$ is low and the second one generates the synchronization pulse. The minimum SYNC input level is 5 volts, which can be generated from a CMOS one-shot or a TTL device with a pull-up resistor. When not used, the sync input should be grounded.

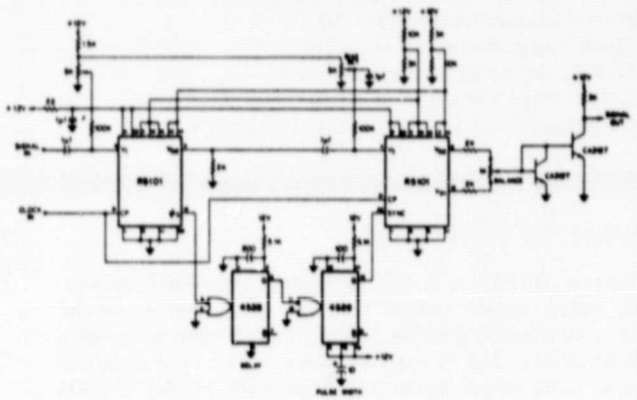


Figure 4. Typical circuit for cascading R5101 devices.

FUNCTION	SYMBOL	PARAMETER			UNITS
		MIN.	TYPICAL	MAX.	
Clock Voltage	V_{CP}	5		VDD	Volts Peak
Sync Pulse Voltage	V_{SYN}	5	10	VDD	Volts Peak
Output Bias	V_{OG}	1	3	4	Volts dc
Corner Bias	V_{CB}	1	3	4	Volts dc
Input Isolation Bias	V_{IG}		3		Volts dc
Analog Input Bias	V_I	3		6	Volts dc*
Signal V_{DD} Voltage	V_{DDS}		12	15	Volts dc
Driver V_{DD} Voltage	V_{DDD}		12	15	Volts dc
Signal V_{DD} Current	I_{DDS}		8		ma
Driver V_{DD}Current	I_{DDO}		8		ma
Reset Drain Voltage Odd	V_{RDO}		9		Volts dc
Reset Drain Voltage Even	V_{RDE}		9		Volts dc
Reset Drain Current Odd	I_{RDO}		70		μamp
Reset Drain Current Even	I_{RDE}		70		μamp
Clock output	$\emptyset_3$				See Fig. 5
Signal Outputs	V_{01} and V_{02}				See Fig. 6
Clock Input Capacitance	CP		4		pF
Analog Input Capacitance	V_I		4		pF

**See text under Applications, for optimum bias adjustment.*

TIME SYMBOL	MIN.	TYPICAL	MAX.	UNITS
t_D	50	100	150	nanosec
t_{DS}	100			nanosec
t_{sample}		100		nanosec
t_{RS}		150		nanosec
t_{FS}		150		nanosec

Table for Timing Diagram.

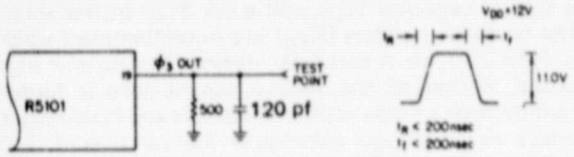


Figure 5. ϕ_3 Output at Maximum Permissible Loading.

ELECTRICAL SPECIFICATIONS

I/O specifications are listed in the Table on the preceding page: All input terminals (with the exception of V_{DD} and V_{RD} are gate inputs of an MOS device, therefore essentially capacitive. Protection is provided on all inputs against damage by static charge; however, the normal precautions applicable to MOS devices should be followed.

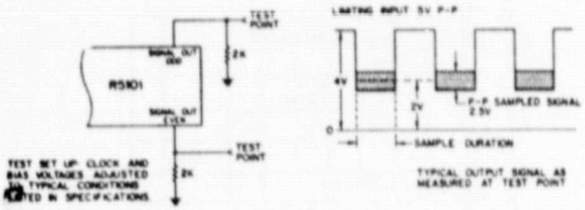


Figure 6A. Signal Output.

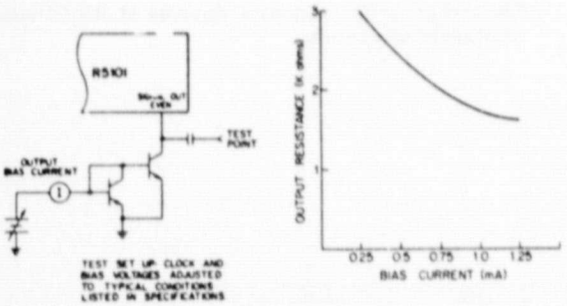


Figure 6B. Output Impedance.

PERFORMANCE CHARACTERISTICS

PARAMETERS	LIMITS MIN.	LIMITS TYPICAL	LIMITS MAX.	UNITS
Sample frequency	0.004		2	MHz
Dynamic Range		See Fig. 7		
Noise		See Fig. 7		
3db Bandwidth (see Fig. 8)	12.5	14		% of frequency sample
Transfer Gain		0.6		Volts/Volt*
Distortion at 1V p-p input		1		%

**The transfer gain was measured with test circuit conditions as shown in Fig. 6A.*

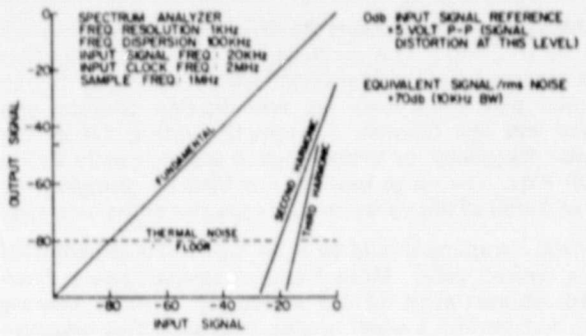


Figure 7. Transfer Characteristic.

APPLICATION

A circuit schematic is shown in Fig. 9 to provide the user with a rapid evaluation of the device. This circuit provides the clock and the biases for the device. It contains an output adder amplifier, CA3127; filter amplifier, 4739; oscillator, one-half of 4013; and a square-wave clock generator, other half of 4013. A circuit similar to the one in Fig. 9 is available on a circuit card from Reticon. Its designation is RC5101.

The circuit is operated from a single power supply of 12 volts at 60 ma. The mid-frequency gain is approximately 0.5. The cutoff frequency of the filter is approximately 20 KHz. As seen in the schematic, there are three potentiometers: (1) input signal bias control, (2) odd and even gain, and (3) frequency control.

The input signal bias control is used to obtain the specified bias setting at the input; however, it may be used to optimize the bias condition by inputting a sine wave of 2 volts p-p signal at 2 KHz and adjusting the potentiometer to obtain an output signal at Pin 8 or 12 with a minimum distortion.

The odd and even gain control is used to adjust the gain differential between the two sides. This is performed by applying a sine wave of ≅ 2 volts to the input and adjusting for balanced gain through the signal swing of the combined output.

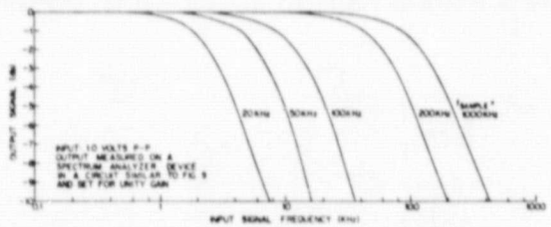


Figure 8. Typical Frequency Response with Various Sampling Frequencies.

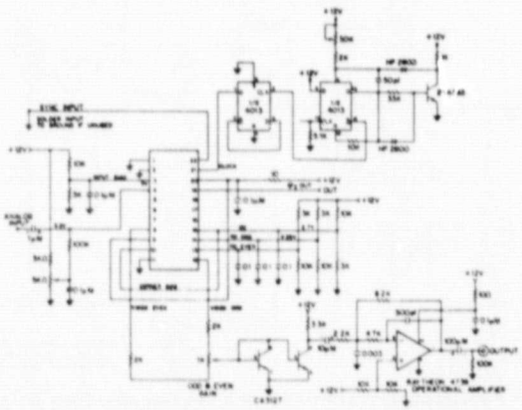


Figure 9. Typical External Circuit for Control of R5101.

The frequency control adjusts the driving oscillator frequency from .02 to 2 MHz. This oscillator drives the 4013 flip-flop which generates the external square-wave clock input. It is to be noted that since there are two flip-flop dividers, one external and one internal, the sampling rate is 1/4 of the oscillator frequency, or in the range of approximately 5 KHz to 500 KHz. The range may be modified by changing the value of the 50-pf frequency-control capacitor at the oscillator.

In general, sampling should be at as high a rate as permitted by the desired delay. More frequent samples give a finer-grained representation of the analog signal, make filtering easier, and permit a wider analog passband. This situation holds true until sampling rate becomes so high that there is insufficient time per sample to readjust charges internally, meaning that sampling rates must be 1 MHz or higher before significant limitations are observable.

Attempts to obtain very long delays face two limitations: (1) The very low sample rate means coarse-grained representation of the analog signal, and a restricted bandwidth. A maximum bandwidth of less than $f_{sample}/2$ obtains, because filters are not ideal; otherwise interference occurs from the folded components ($f_{sample} - f_{signal}$). (2) Storage time is limited by internal leakage current. Leakage is worse at high operating temperatures, doubling every 7–10°C increase in temperature. The leakage affects bias levels and introduces noise, because of the additive nature of the leaked charge.

FREQUENCY COMPENSATION CIRCUIT

The bandwidth of an ideal device would be limited by sampling considerations. Input frequencies must be limited to less than half the sample frequency and filtered outputs will have a SIN X/X envelope. In a real charge transfer device there is an additional factor which comes from the charge transfer inefficiency; that is, some signal charge is left behind at each transfer and comes out as a trailing signal. The exact amount of transfer inefficiency varies from device to device. The block diagram for a circuit which compensates for this and which tracks with changes in the sample frequency is shown in Figure 10. The concept for this type of sampled data filter circuit is that it cancels the trailing signal which comes out during sample periods later than the one to which it belongs. With a single loop (n=1), the circuit only cancels the trailing charge in the next sample period. In the detailed circuit shown in Figure 12, n=2 and this allows the 3db point of the R5101 to be set at .25 f sample. Figure 11 shows the output of an R5101 device uncompensated and compensated in the circuit of Figure 12.

In the Figure 12 circuit each S/H of the block diagram is realized with two sections, each section produces one-half sample of delay. A section consists of a SD5000 switch, a .001 μ storage capacitor (C_S), and a CA 3127 buffer amplifier. The feedback resistors (R_{Fn}) are potentiometers which can be optimized for a particular device. The output from the second section of the second sample-hold is further processed through a single additional sample and hold section to produce an optimized rectangular box-car output. This circuit will produce slightly more noise than the circuit of Figure 9 as the high frequency noise is peaked as well as the signal.

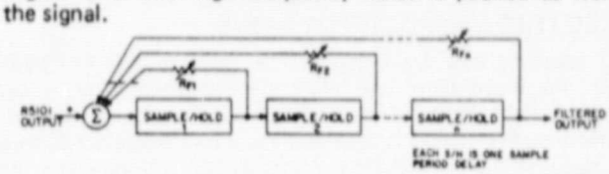


Figure 10. Block diagram for n loop sampled data filter.

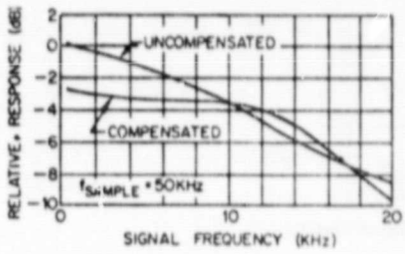


Figure 11. Comparison of the frequency response of R5101 using different output circuits.

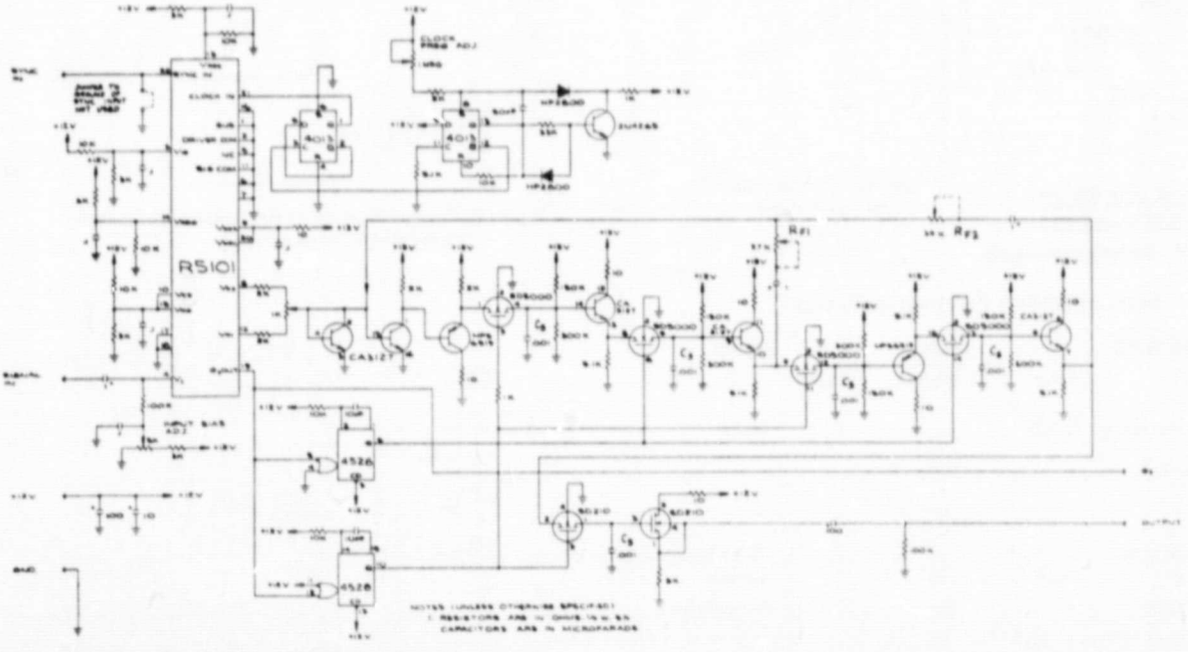


Figure 12. Typical circuit for R5101 with sampled data filter output.

GENERAL DESCRIPTION—The CCD321A is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321A consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

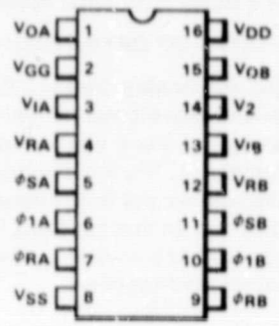
The CCD321A can be used in applications ranging from video frequencies all the way down to audio frequencies. A complete TV line of 63.5 μs can be stored with a four times color subcarrier sampling frequency of 14.318 MHz. Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321A also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.

The CCD321A is an improved pin-for-pin replacement for the CCD321. The CCD321A comes in four different classes as follows:

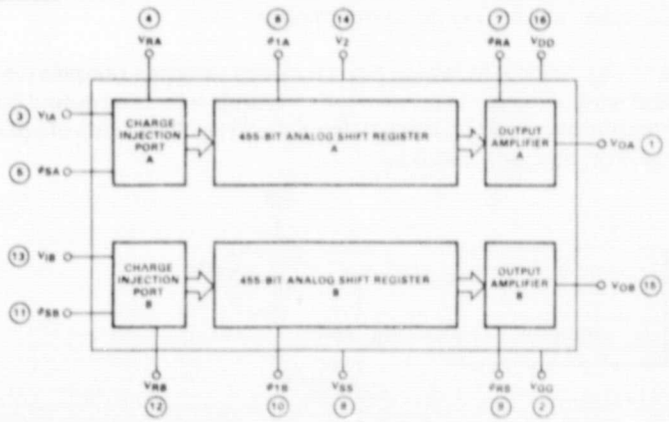
DEVICE	APPLICATION
CCD321A-1	Broadcast quality video delay line
CCD321A-2	High quality video delay line
CCD321A-3	Time base compression and expansion delay line
CCD321A-4	Audio delay line

- **ELECTRICALLY VARIABLE ANALOG DELAY LINE FOR AUDIO AND VIDEO APPLICATIONS**
- **1 H VIDEO DELAY LINE CAPABILITY WITH BROADCAST QUALITY PERFORMANCE.**
- **EXCELLENT BANDWIDTH AT VIDEO AND AUDIO RATES DUE TO BURIED CHANNEL TECHNOLOGY.**
- **WIDE RANGE OF DATA RATE: FROM 10 MHz TO 20 MHz PER 455 SECTION.**
- **HIGH SIGNAL TO NOISE RATION—VIDEO: 58 db, AUDIO: 65 db.**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES	
Φ_{1A},Φ_{1B}	Analog Shift Register Transport Clocks
Φ_{SA},Φ_{SB}	Input Sampling Clocks
Φ_{RA},Φ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA},V_{IB}	Analog Inputs
V_{RA},V_{RB}	Analog Reference Inputs
V_{OA},V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

 Printed in U.S.A./254-11-0004-127/15M

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

FUNCTIONAL DESCRIPTION — The CCD321A consists of the following functional elements illustrated in the Block Diagram:

Two Charge Injection Ports — The analog information in voltage form is applied to two input ports at V_{IA} (or V_{IB}). Upon the activation of the analog sample clocks ϕ_{SA} (or ϕ_{SB}) a charge packet linearly dependent on the voltage difference between V_{IA} and V_{RA} (or V_{IB} and V_{RB}) is injected into analog shift register A (or B).

Two 455-Bit Analog Shift Registers — Each register transports the charge packets from the charge injection port to its corresponding output amplifier. Both registers are operated in the 1-1/2 phase mode where one phase (ϕ_{1A} or ϕ_{1B}) is a clock and the other phase (V_2) is an intermediate dc potential. Phases ϕ_{1A} and ϕ_{1B} are completely independent. V_2 is a dc voltage common to both registers.

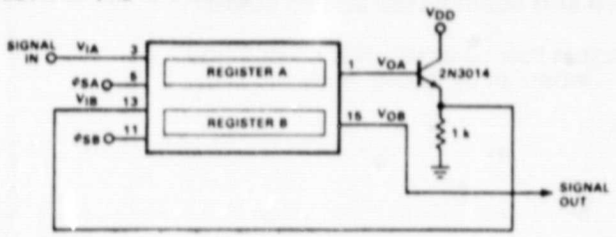
Two Output Amplifiers — Charge packets from each analog shift register are delivered to their corresponding output amplifier as shown in the circuit diagram. Each output amplifier consits of three source follower stages with constant current source bias. A sample and hold transistor is located between the second and third stage of the amplifier. When the gate of the sample and hold transistor is clocked (ϕ_{RA} or ϕ_{RB}) a continuous output waveform is obtained as shown in the timing diagrams. The sample and hold transistor can be defeated by connecting ϕ_{RA} and/or ϕ_{RB} to V_{DD}. In this case the output is a pulse modulated waveform as shown in the timing diagram.

MODES OF OPERATION — The CCD321A can be operated in four different modes:

455-Bit Analog Delay — Either 455-bit analog shift register can be operated independently as a 455-bit delay line. The driving waveforms to operate shift register A is shown in Fig. 10. The input voltage signal is applied directly to V_{IA}. The input sampling clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of register A. The input voltage A_1 which is sampled between $t = 0$ and $t = t_c$ appears at the output terminal V_{OA} at $t = 910t_c$. If the sample and hold circuit is not used then the output appears as a pulse amplitude modulated waveform as shown in the diagram. In that case ϕ_{RA} (pin 7) should be connected to V_{DD} (pin 16). If the sample and hold circuit is used than the output appears as a continuous waveform. Here ϕ_{RA} (pin 7) should be clocked coincident with ϕ_{SA} (pin 5) and the two pins can be connected together.

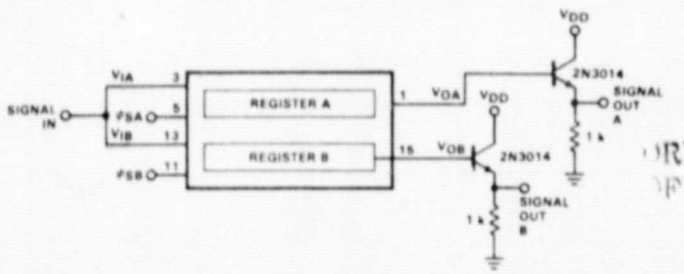
Analog shift register B can be operated in an analogous manner with V_{IB} as the analog input, ϕ_{1B} as the transport clock, ϕ_{SB} as the input sampling clock and ϕ_{RB} as the output sample and hold clock.

910-Bit Analog Delay In Series Mode — The two analog shift registers A and B can be connected in series to provide 910 bits of analog delay as shown in the schematic below. The analog signal input voltage is applied to V_{IA}. The output of register A is connected to the input of register B with a simple emitter follower buffer stage. In order to insure proper charge injection of register B, V_{RB} should be adjusted. The timing diagram shown in Fig. 10 applies in this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{SA} = \phi_{SB}$, $\phi_{RA} = V_{DD}$, and ϕ_{RB} is clocked.



910-Bit Analog Delay In Multiplex Mode — The two analog shift registers can be connected in parallel to provide 910-bit of analog delay as shown in the schematic below. The analog signal input voltage is applied to both V_{IA} and V_{IB}. The outputs at V_{OA} and V_{OB} should be combined in order to recover the analog input information.

The necessary waveforms to operate the device in this mode is shown in Fig. 11. In this case ϕ_{SA} samples the analog input A_1 at V_{IA} between $t = 0$ and $t = t_c$. ϕ_{SA} samples the analog input B, at V_{IB}, between $t = t_c$ and $t = 2t_c$. The output corresponding to A_1 appears at V_{OA} at $t = 910t_c$. The output corresponding to B_1 appears at V_{OB} at $t = 911t_c$. This mode of operation results in an effective sampling rate of twice the rate of ϕ_{1A}, ϕ_{1B}, ϕ_{SA} and ϕ_{SB}.



Stop/Start Mode Operation — The charge packets in the two analog shift registers can be held stationary by stopping ϕ_{1A} and ϕ_{1B} in their LOW state ϕ_{SA}, ϕ_{SB}, ϕ_{RA}, and ϕ_{RB} can also be stopped in the LOW state or kept clocking as usual. The two shift registers should not be connected in series in the stop-start mode of operation.

The CCD321A comes in four different classes depending on the particular application. The CCD321A-1 is basically a high quality broadcast 1 H delay line for video systems with 1% differential gain and 1° differential phase. The CCD321A-2 is a high quality video delay line with 3% differential gain and 3° differential phase. The CCD321A-3 is tested in the START/STOP mode of operation and parameters guaranteed in this mode. The CCD321A-4 is tested at audio speeds and audio type parameters are specified and guaranteed. The dc and clock characteristics of the four classes are the same. The ac characteristics vary as shown below.

Caution: The device has limited built-in gate protection. Charge build-up should be minimized. Care should be taken to avoid shorting pins V_{OA} and V_{OB} to ground during operation of the device.

DC CHARACTERISTICS: $T_A = 55°C$, Note 16

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{DD}	Output Drain Voltage	14.5	15.0	15.5	V	
V_2	Analog Shift Register DC Transport Phase Voltage		6.0		V	Note 1
V_{RA},V_{RB}	Analog Reference Inputs Voltage		3-7		V	Note 2
V_{GG}	Signal Ground		0.0			
V_{SS}	Substrate Ground		0.0			Note 3
R_{IN}	AC Input Resistance		1.0		MΩ	Resistance from Pins 3, 4, 12 or 13 to V_{SS}. $V_{IA} = V_{IB} = 3$ V
C_{IN}	AC Input Capacitance		10		pF	Capacitance from Pins 3, 4, 12 or 13 to V_{SS}. $V_{IA} = V_{IB} = 3$ V
R_{OUT}	AC Output Resistance		250		Ω	$V_{DD} = 15$ V

CLOCK CHARACTERISTICS: $T_A = 55°C$, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V\phi_{1AL}$, $V\phi_{1BL}$	Analog Shift Register Transport Clocks LOW	0	0.5	0.8	V	Note 4
$V\phi_{1AH}$, $V\phi_{1BH}$	Analog Shift Register Transport Clocks HIGH	12.0	13.0	15.0	V	Note 4
$V\phi_{SAL}$, $V\phi_{SBL}$	Input Sampling Clocks LOW	0	0.5	0.8	V	Note 5
$V\phi_{SAH}$, $V\phi_{SBH}$	Input Sampling Clocks HIGH	12.0	13.0	15.0	V	Note 5
$V\phi_{RAL}$, $V\phi_{RBL}$	Output Sample and Hold Clocks LOW	0	0.5	0.8	V	Note 6
$V\phi_{RAH}$, $V\phi_{RBH}$	Output Sample and Hold Clocks HIGH	12.0	13.0	15.0	V	Note 6
V_{IA}, V_{IB}	Input DC Level		3-7		V	Note 2
V_{OA}, V_{OB}	Output DC Level		6-11		V	$V_{DD} = 15$ V
$f\phi_{1A}$,$f\phi_{1B}$	Analog Shift Register Transport Clock Frequency	0.02		20	MHz	See Note 17
$f\phi_{SA}$,$f\phi_{SB}$	Input Sampling Clocks Frequency	0.02		20	MHz	See Note 17
$f\phi_{RA}$,$f\phi_{RB}$	Output Sample and Hold Clocks Frequency	0.02		20	MHz	See Note 17
ODM	Output DC Mismatch Between A & B Registers		±1		V	
OAM	Output AC Mismatch Between A & B Registers		±20		%	

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
All Pins with Respect to V_{SS}	−0.3 V to 20 V

CCD321A-1 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz. Sampling Rate = 14.32 MHz. Vout = 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	5.0			MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			1.0	%	Note 9
Δ ϕ	Differential Phase			1.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-2 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Vout = 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-3 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplied mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Clocks are stopped for 300 μs. Vout = 700 mV after 4.2 MHz low pass filter. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	**Differential Gain**			**3.0**	**%**	**Note 9**
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	55			dB	Note 10
SN	Spacial Noise		10.0	20.0	mV	Note 11, 12
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-4 AC CHARACTERISTICS: $T_A = 45°C$. For each register, Data Rate = 50 KHz. (See Test Load Configuration, Figure 9)
Vout = 1 V

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	23	25		KHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
THD	Total Harmonic Distortion		0.5	1	%	Note 13
S/N	Signal-to-Noise Ratio	60	65		dB	Note 14
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	
RSO	Rate of Average Signal Offset		15		mv/ms	Note 15

NOTES:
1. V_2 level should be 1/2 of the ϕ_{1A} or ϕ_{2A} HIGH level. Adjustment in the range of ±1 V may be necessary to maximize signal bandwidth.
2. Signal charge injection is proportional to the difference V_I and V_R. Adjustment of either V_I or V_R is necessary to assure proper operation.
3. Negative transients below ground of fast rise and fall times of the clocks may cause charge injection form substrate to the shift registers. A negative bias on V_{SS} of -2.0 to -5.0 Vdc will eliminate the injection phenomenon.
4. $C\phi_{1A} = C\phi_{1B} = 30$ pF = Capacitance with respect to V_{SS}.
5. $C\phi_{SA} = C\phi_{SB} = 10$ pF = Capacitance with respect to V_{SS}.
6. $C\phi_{RA} = C\phi_{RB} = 10$ pF = Capacitance with respect to V_{SS}.
7. Signal Bandwidth is typically 1/3 to 1/2 of the sampling rate. See Fig. 1.
8. Insertion Gain = 20 Log V_{OUT}/V_{IN}
9. Differential Gain and Differential Phase are measured with Tektronix NTSC Signal Generator (147A) and Vector Scope (520A). See Figure 2.
10. Video S/N is defined as the ratio the peak-to-peak output signal to RMS random (temporal) noise. The peak-to-peak signal is the maximum output level that satisfies the ΔG and $\Delta\phi$ specs. See Fig. 3.
11. In the start/stop mode of operation it is recommended that the rise and fall times of ϕ_{1A} and ϕ_{1B} exceed 20 ns to eliminate charge injection.
12. Spacial Noise is the peak-to-peak spacial variation (fixed pattern noise) in the device output after clocks have been stopped. It is usually caused by the variation of leakage current density in the shift registers. Spacial noise is a function of the clock stop period and temperature. See Figure 5.
13. Input Signal = 1KHz sine wave. See Figure 6.
14. Audio S/N is defined as the ratio of RMS noise at 23 KHz bandwidth. Both are measured with an HP3400A RMS Voltmeter. See Figure 6.
15. Rate of Average-Signal Offset is caused by leakage current in the registers. It is a function of temperature. See Figure 7.
16. Devices are tested using the values shown in the typical columns.
17. Devices can be operated beyond 20 MHz without damage. The minimum clock rate can be lower than 10 KHz shown in Figure 4.

TYPICAL VIDEO PERFORMANCE CURVES

FREQUENCY RESPONSE (FOR SINGLE REGISTER)

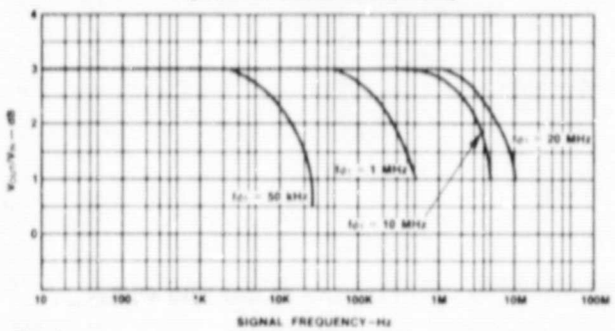


Fig. 1

DIFFERENTIAL GAIN AND PHASE VERSUS OUTPUT VOLTAGE

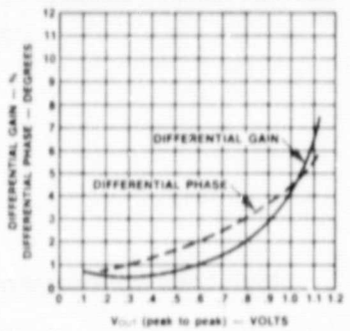


Fig. 2

DIFFERENTIAL GAIN AND PHASE VERSUS S/N RATIO

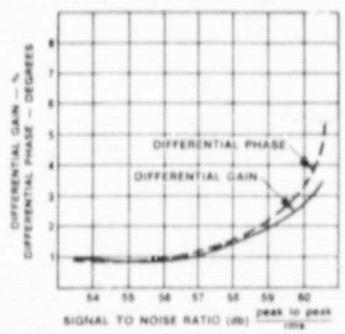


Fig. 3

V_{OUT} MAX VERSUS CLOCK FREQUENCY

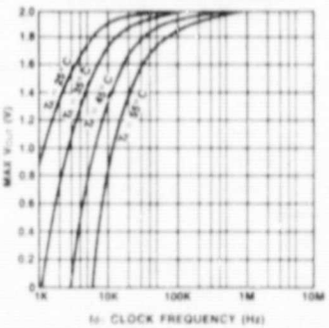


Fig. 4

SPACIAL NOISE VERSUS CLOCK STOP PERIOD

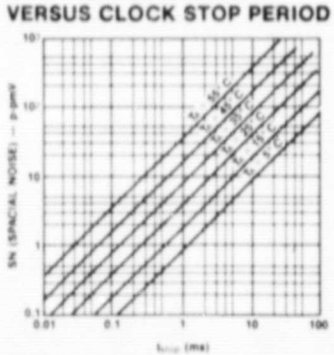


Fig. 5

App. 3-5

TYPICAL AUDIO PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION (THD) AND S/N RATION VERSUS V_{OUT}

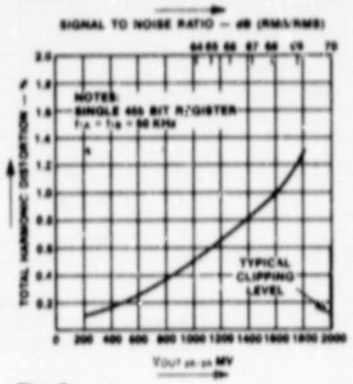


Fig. 6

RATE OF AVERAGE SIGNAL OFFSET VERSUS TEMPERATURE

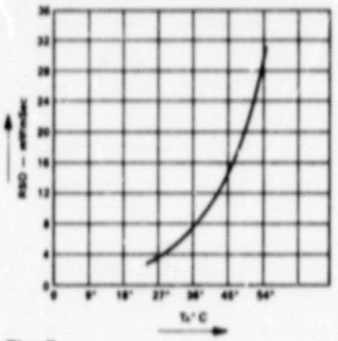


Fig. 7

TEST LOAD CONFIGURATION FOR MILTIPLEXED OPERATION IN VIDEO

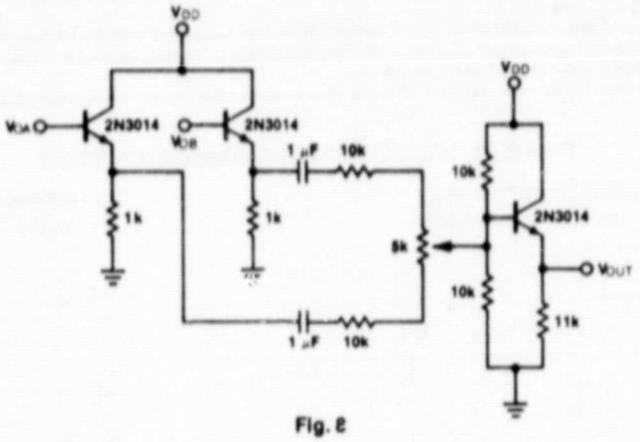


Fig. 8

TEST LOAD CONFIGURATION FOR SINGLE REGISTER OPERATION IN AUDIO AND VIDEO

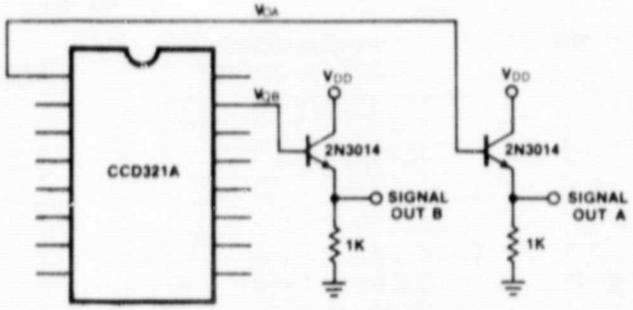
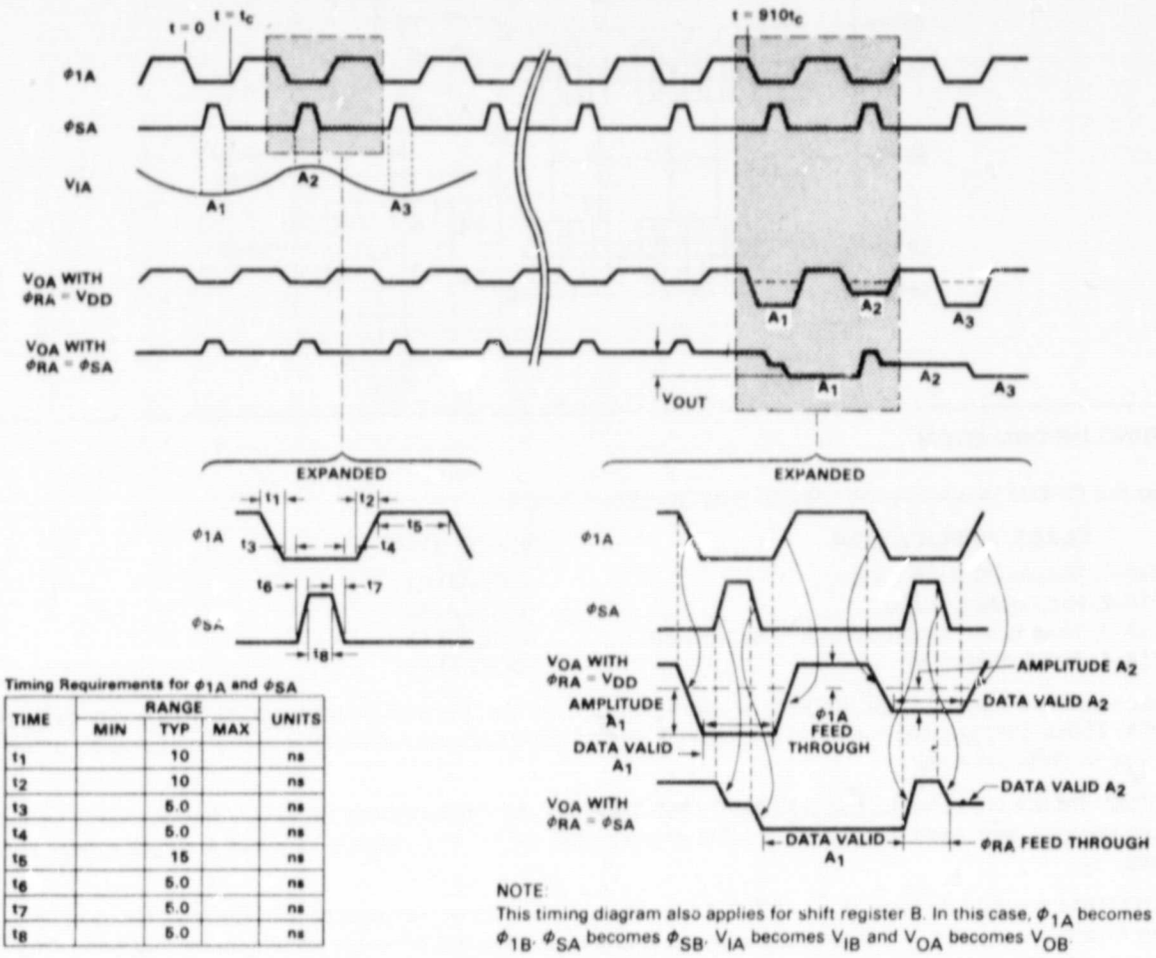


Fig. 9

TIMING DIAGRAM



Timing Requirements for ϕ_{1A} and ϕ_{SA}

TIME	RANGE			UNITS
	MIN	TYP	MAX	
t_1		10		ns
t_2		10		ns
t_3		5.0		ns
t_4		5.0		ns
t_5		15		ns
t_6		5.0		ns
t_7		5.0		ns
t_8		5.0		ns

NOTE:
This timing diagram also applies for shift register B. In this case, ϕ_{1A} becomes ϕ_{1B}, ϕ_{SA} becomes ϕ_{SB}, V_{IA} becomes V_{IB} and V_{OA} becomes V_{OB}.

Fig. 10 Analog Shift Register A or B Operation

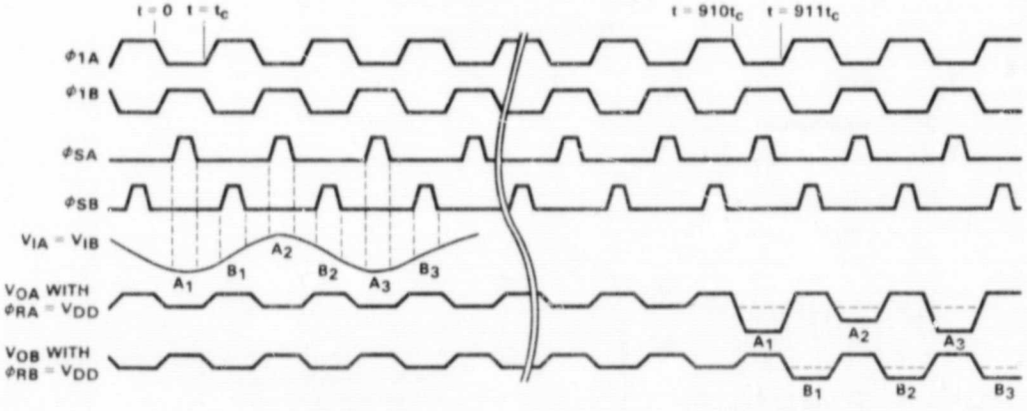
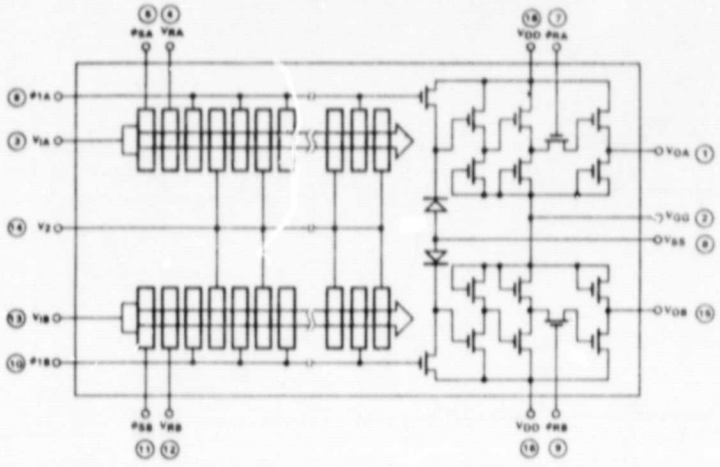


Fig. 11 Analog Shift Register A and B Operation in the Multiplexed Mode

Fig. 12 Circuit Diagram



ORDERING INFORMATION

To order the CCD321A specify the "device type" as shown below:

CLASS, APPLICATION	DEVICE TYPE
CCD321A-1, Broadcast quality video	CCD321A1
CCD321A-2, High quality video	CCD321A2
CCD321A-3, Time base compression and expansion	CCD321A3
CCD321A-4, Audio delay line	CCD321A4

Also available from Fairchild are two fully assembled modules that contain all the necessary circuitry to operate the CCD321A. These modules are designed to help the system designer become familiar with the operation of the device, and for use in OEM systems.

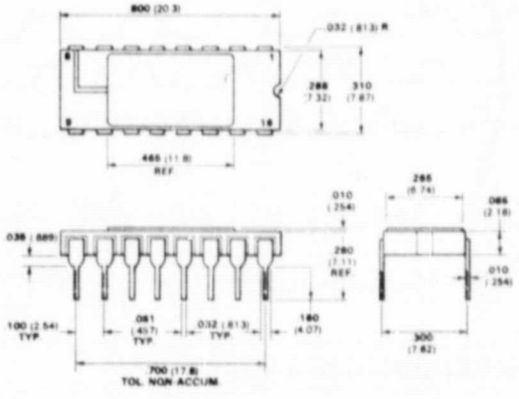
The CCD321VM is a video module using a CCD321A-3. The module includes the necessary electronics to perform time base compression and expansion, and variable video signal delay. The module requires a single power supply for operation.

The CCD321AM is a module using three CCD321A-4 which are connected in series to provide delay times of up to 100 ms for audio frequency signals. A filtered output tap is provided at each 455 bit delay increment for flexibility. The module requires a single supply for operation.

Schematics and component layouts are included in the shipping packages for the CCD321VM and CCD321AM. For further information on the CCD321VM or CCD321AM please contact your nearest Fairchild sales office or distributor or call 415-962-3941.

PACKAGE OUTLINE

16-Pin Side Brazed



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Header is black ceramic (Al_2O_3)
Pins are gold-plated kovar
Top cover connected to pin 8 (V_{SS} substrate)